APPENDIX A

Low Cost Ultra-Low On-Resistance High-Current Switching MOSFET for Low Voltage Power Conversion

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Summary of Invention:

The use of diodes for output current rectification in low output voltage switching power converters or power supplies is precluded by the severe loss in efficiency due to the forward voltage drop of diodes becoming comparable to the desired output voltage, V_{out}, of the converter. The use of MOSFETs or other similar high-current switching devices in a synchronous rectifier approach can overcome this efficiency problem if the "on" resistance, R_{on}, of the current switching MOSFETs is sufficiently low to make the $I_{out}R_{on}$ voltage drop of across the switches much lower than V_{out}. This can be achieved with conventional MOS power FETs by making the FET periphery (total channel width, W) very large, either by making one very large device, or by connecting many smaller devices in parallel. In either approach, to achieve very low R_{on} values, the device cost becomes quite large due to the large size of a single die, or the large number of paralleled devices. Also, the total gate capacitance of all of these devices becomes very large, which limits the attainable switching speed and causes significant losses in converter efficiency due to the large ac gate drive power requirements.

Aspects of the present invention take advantage of the fact that in a switching converter application, the breakdown voltage, V_b, required for the synchronous rectifier switching devices is, for an output voltage of V_{out}, only about $V_b=2V_{out}$. For example, for an output voltage of $V_{out}=1.2V$, a breakdown voltage of about $V_b=2V_{out}=2.4V$ is adequate for the synchronous rectifier MOSFET switches. In aspects of this invention, this low breakdown voltage requirement is exploited to enable implementation of the synchronous rectifier switching MOSFETs with an inexpensive commercial deep-submicron CMOS integrated circuit foundry process (instead of the special higher voltage process normally used for fabricating power MOSFET devices). For a given R_{on}, compared to standard MOS power FET processes, the use of a very short channel length (e.g., $L_{eff}=0.19\mu m$)/very small feature size (e.g., $2\lambda=0.24\mu m$) commercial IC process for fabricating the current switches dramatically reduces the size and cost of the devices, and also greatly reduces the gate capacitance and increases switching speeds for higher efficiency and smaller converter size.

The dramatic size/cost reduction comes through the combined effect of a reduction in the MOSFET periphery, W, required to achieve a given value of R_{on} (because of the very small L_{eff}), with the fact that the very small feature size allows packing a given MOSFET periphery into a much smaller chip area. For example, at the silicon device level, an extremely low "on" resistance of less than $R_{on}=75\mu\Omega$ can be achieved for a 200 amp switching MOSFET with a total $L_{eff}=0.19\mu m$ FET

periphery of less than W=13.5 meters, and with a 2λ=0.24μm feature size, this W=13.5 meter MOSFET can be packed into a chip only 4mm x 4mm in dimensions. At an estimated foundry CMOS foundry wafer cost of $1500 per 8" (200mm) wafer, the unpackaged die cost for such a 200 amp switching MOSFET chip should be less than $1.00. This deep-submicron approach gives not only a much smaller solution to achieving an extremely low R_{on} 200 amp current switching MOSFET, but promises to be 10x to 100x cheaper than implementations using standard power MOSFET processes. In addition, because of the reduced FET periphery and very short (L_g=0.24μm drawn) gate length, the gate capacitance is far lower, and the switching speed much higher than in the power MOSFET implementation, and the ac gate drive power at a given switching frequency can be reduced by nearly a factor of 500 over conventional vertical geometry power MOSFETs.

Also important to some aspects of this invention is the solution of the problem of getting such large (e.g., 200 amp) currents into and out of the small (e.g., 4 mm x 4 mm) FET chip without encountering metal migration reliability problems or unduly compromising R_{on} from the on-chip metal resistance or package resistance. Conventional power MOSFETs take the source and drain currents out of opposite faces of the die (e.g., all of the area devoted to source contacts, plus the gate leads, are on the top surface of the die, while the drain contact is the entire back surface of the die. Having the high-current source and drain contacts on opposing surfaces of the die makes the die packaging/interconnect quite easy. A disadvantage of using a CMOS integrated circuit process instead of a power MOSFET process is the unavailability of this backside drain contact configuration. The MOSFET geometries in commercial CMOS IC processes are purely lateral; that is a source-gate-drain electrode structure on the top surface of the semiconductor die. Hence, in order to implement aspects of this invention and use a commercial deep-submicron CMOS process to make the low R_{on} current switching MOSFETs, we have to be able to get both the high current source and drain contacts (plus one or more gate leads) off of the same (top) surface of the die. The key to the solution of this high-current chip packaging/interconnect interface problem is to cover at least substantially the entire area of the die with a fine pitch area array of solder bump contacts which flip-chip mate with a matching array on a very low resistance multi-layer metal package. It is desirable that the pitch of these solder bump contacts be as low as possible to minimize the metal resistance. While a standard commercial practice area array bump pitch of 250μm is adequate to give a total (i.e., silicon FET + on-chip metal + solder bump + package metal) resistance of the order of 285μΩ, with a smaller, 100μm bump pitch (which is also commercially available), the total R_{on} can be reduced to less than 180μΩ for the MOSFET chip example cited above. This very low resistance is a result of the sharing of the source and drain current by a large number of solder bump contacts (e.g., 126 bumps each for the 250μm pitch and about 800 bumps each for the 100μm pitch, which accounts for its better R_{on} performance).

In summary and in accordance with exemplary aspects of the invention, the use of a commercial deep-submicron CMOS integrated circuit process in conjunction with an area array solder bump flip-chip packaging approach allows the achievement

of high-current (e.g. 200 amp), very low on resistance low voltage MOSFETs having much lower cost and much lower gate capacitance, not to mention much smaller size, than devices implemented using conventional power MOSFET processes.

Background of Invention

A key focus of modern digital electronics is to achieve extremely high computational densities; that is, to cram as much computational throughput as possible into a limited space. The relationship between something as seemingly tenuous or intangible as computational power and a simple concrete physical quantity like dc power input or waste heat generated may not be obvious. In fact, computational throughput ("power") is, as a matter of physics, tied to the conversion of dc input supply power to heat. Moreover, in the most efficient forms of logic circuitry, the level power consumption/heat generation is essentially proportional to the computational throughput, albeit the exact value of the constant of proportionality is dependent on details of the integrated circuit (IC) technology used to implement the computer. Specifically, it can be shown that for CMOS logic (in which the dynamic power dissipation dominates), a chip with N_g gates, each driving an average load capacitance, C_{gl}, operating at a supply voltage, V_{dd}, and at a clock frequency, F_c, with a fraction, f_d, of those gate switching on each clock cycle, the chip power, P_d, will be given by

$$P_d = {}^1/_2\, f_d\, N_g\, C_{gl}\, V_{dd}^2\, F_c \qquad \text{Eq. 1}$$

Since a reasonable measure of computational activity is the number of such logic gates that have switched, the measure of computational throughput (rate) is simply the number of such logic gates switching per unit time, $f_d N_g F_c$, or

$$\text{Computing Rate} \propto f_d\, N_g\, F_c = P_d \,/\, [{}^1/_2\, C_{gl}\, V_{dd}^2] \propto P_d \qquad \text{Eq. 2}$$

which shows the (technology dependent) proportionality between computational throughput and the power consumed (dissipated). What this means is that the quest for high computational density forces designers to cope with both high power supply densities, as well as the ability to handle high reject heat densities.

Advances in integrated circuit technologies, principally through the reduction in lithographic feature sizes and FET gate lengths into the deep submicron region, have made it possible to put millions of logic gates on a single monolithic IC chip, as well as to increase clock rates, F_c, into the 500 MHz to 1 GHz region. This means, from Eq. 2, that since both n_g and F_c have been increased, remarkably high computational throughputs can be achieved even on a single chip microprocessor. While feature size reductions also serve to reduce CMOS FET gate capacitances (C_{gs} and C_{gd}), much of the gate loading capacitance, C_{gl} in Eqs. 1 and 2, is due to interconnect wire capacitance, which is principally a function of wire length, and hence does not scale strongly with feature size. This means that if the logic power

supply voltage were held constant, the chip dissipations would become astronomical (e.g., many kilowatts) for these very dense, high throughput chips. This problem has been recognized by the semiconductor industry, and as a consequence the power supply voltages have been gradually reduced over the last decade from their original V_{dd}=5.0 V level down to Vdd=1.2 V for the latest 2λ=0.24 μm feature size, L_{eff}=0.19 μm gatelength CMOS logic.

While this reduction on V_{dd} has helped keep chip power dissipations to a manageable level (typically under 100 W to 200 W per chip), which helps the thermal management problem, in fact it has in some ways made the power supply/distribution problem even more difficult. The problem is that while the chip power requirements have been maintained at tolerable levels, the power supply current requirements have increased sharply, while at the same time the tolerance for IR voltage drops in the power distribution conductors has become more severe. For example, consider a logic power (in one or more chips) requirement of P_d=240 W. In the "old days" of V_{dd}=5 V logic, from $P_d=V_{dd}I_s$, the required supply current would be I_s=240/5=48 amps, and for a 10% dc noise margin allowable $V_{ndc}=I_sR_s$=0.5 V drop, the allowable wiring resistance between the power supply and the logic is R_s=0.5/48=10.4 mΩ. With the reduced V_{dd}=1.2 V logic, the required supply current would be I_s=240/1.2=200 amps, and for a 10% dc noise margin allowable $V_{ndc}=I_sR_s$=120 mV drop, the allowable power distribution resistance from supply to logic is only R_s=0.12/200=600 $\mu\Omega$. It is probably obvious that it is <u>very</u> difficult to achieve such low power distribution resistances. While it is correct that the use of an on-board regulator near the logic chips could make it much easier to meet the dc noise margin requirements of the logic, note that at I_s=200 amps, even a R_s=1.0 mΩ wiring resistance (including the regulator resistance) between the power supply and the logic chips will reduce the power efficiency by over 14%, so sub-millivolt resistances are indeed required. Conventional circuit board connectors, etc., are not capable of handling 200 amp currents with sub-millivolt resistances, so another approach is needed.

The most attractive approach to solving this problem is to distribute the power to the boards at a high voltage (e.g., V_{in}=48 volts), using very efficient on-board power converters to convert this to the V_{dd}=1.2 volt logic supply level. In order to insure that the on-board power conversion does not unacceptably compromise the overall density of the electronics, it is desirable to make the on-board power converter as small as possible. In a switching converter, the stored energy requirements in the magnetics (e.g., transformers and inductors) and in bypass or filter capacitors can be reduced by increasing the switching frequency, f_s, of the converter. This is difficult, however, because of the limited switching speeds of most semiconductor devices capable of handling large currents. Addressing this deficiency is one focus of aspects of this invention; that is to provide low cost MOSFET switches capable of handling high currents at high switching speeds.

While the use of on-board power conversion to efficiently supply low voltage logic requirements in high-performance systems is extremely attractive, there is an

inherent difficulty with achieving high efficiency, very small low voltage power converters. The ordinary method of building a switching converter involves a transformer to convert down to low voltage ac, with diodes to rectify this to dc. If the forward voltage drop of these rectifier diodes is V_f and the output voltage is V_{out}, then the voltage loss in the diodes alone will limit the attainable rectifier efficiency, η_r, to a value less than

$$\eta_r \leq V_{out}/(V_f + V_{out}) \qquad \text{Eq. 3}$$

Typical Schottky diode forward voltage drops are of the order of V_f=0.55 V or more. In the "old days" of 5 volt supplies, this diode efficiency limit, about η_r=90%, was quite acceptable. With the new low supply voltages, this is no longer the case, as Eq. 3, with V_f=0.55 V, gives a limiting efficiency of about η_r=69% at V_{out}=1.2 volts, or about η_r=62% at V_{out}=0.9 volts. These are unacceptably low values of conversion efficiency.

The solution to this problem is to employ MOSFET current switches in place of the diodes (this approach is called synchronous rectification). If the MOSFET "on" resistance, R_{on}, is sufficiently low, this rectification efficiency loss may be kept very low. Unfortunately, using commercial devices fabricated with the standard vertical "power MOSFET" device structure, to get a low enough R_{on} value, it is often necessary to parallel large numbers of power MOSFET devices in each of the two current switching positions in the circuit. Also, the enormous gate capacitance of all of these power MOSFETs makes gate drive very difficult and causes significant efficiency loss due to $\frac{1}{2}\, C_{gs}\, \Delta V_g^2\, F_c$ gate drive power. This, plus the limited switching speeds of the standard power MOSFET devices, effectively limits the usable switching frequency of the converters. Since the size of the magnetics (and capacitors) goes inversely with the frequency, this makes it very difficult to miniaturize the converters for on-board use (of course, having large numbers of power MOSFETs gives a size problem itself).

Description of Exemplary Aspects of the Invention

Aspects of the invention achieve extremely low R_{on} values and extremely low gate capacitances/high switching speeds in a MOSFET current switching device, including a packaging approach enabling it to be used in circuits. Some concepts of the invention use a completely different device structure from the vertical geometry of power MOSFETs; in fact, to make current switching MOSFETs in a horizontal (planar) geometry using the same 0.25 μm to 0.18 μm CMOS IC processes that are used to fabricate the high-speed logic chips themselves. While the transistors in these deep-submicron short-channel CMOS processes have only about 2.5 - 3 volt breakdown voltages, for a synchronous rectifier having V_{out}=1.2 volt, a V_{br}=2.4 volt breakdown voltage is adequate for the transistors. With this approach, in a chip only 4 mm x 4 mm in size, it is possible to switch currents of 200 amperes and to achieve a value of R_{on} superior to that of the parallel combination of dozens of power

MOSFETs, and at a very small fraction of the gate capacitance. This makes it possible to reduce the ac gate drive power required to switch to a given R_{on} value at a given switching frequency by nearly a factor of 500 over conventional vertical power MOSFETs.

Other aspects of the invention provide a packaging approach capable of getting 200 amperes into and out of such a small chip without substantially degrading the R_{on} value. Whereas the vertical geometry of a conventional power MOSFET has the source lead on the top surface of the die and the drain lead on the bottom, in the horizontal or planar MOSFET structure, the source and drain leads (as well as the gate connection) are on the top surface of the device. On-chip metallization layers on semiconductor die generally have substantial sheet resistances (e.g., 40-80 mΩ/square) and limited current carrying capacity. This makes combining the distributed MOSFET currents from the myriad of elemental MOSFET devices spread over the area of the chip into single source and drain MOSFET chip contacts on the top surface of the die without unacceptably degrading both R_{on} and the current switching capacity of the chip. In aspects of this invention, a solution to this packaging/interconnection problem for current switching MOSFETs fabricated in the horizontal or planar structure is to utilize an area array of a large number (many hundreds to thousands) of chip source and drain contact pads (plus gate pads) covering the top surface of the die. With the very large source and drain currents divided into a large number of parallel paths, the aggregate current carrying capacity can be very large and the metal contribution to the chip on resistance can be small. The area pad array may be flip-chip mated to a mirror-image area pad array in a very low resistance package. A multi-layer package approach utilizing thick copper interconnect layers has been designed to meet the requirements of contacting such an area array planar current-switching MOSFET chip with capability for handling 200 ampere currents with package contribution to total on resistance of less than 100 μΩ.

The achievement of an inexpensive, ultra-low on resistance planar current switching MOSFET is anticipated to have a wide range of applications in addition to efficient low-voltage on-board power conversion. Very low R_{on} MOSFETs could have application in a wide variety of low-voltage high-current applications, ranging from linear applications such as high-current regulators and drivers to switching applications such as efficient high-density power supplies and converters, including solar cell power conversion, and switch-mode drivers for motors and actuators.

<u>Comparison of Device Structure of Aspects of the Invention to Conventional Power MOSFET</u>

The dramatic difference between the horizontal or planar geometry current switching MOSFET structure of aspects of this invention and the vertical geometry of a conventional power MOSFET is illustrated in Figure 1a. Figure 1a shows the device structure of a conventional power MOSFET. In an N-channel device of this

structure, electrons flow from the n^+ diffused source regions horizontally across the p body region (which is electrically shorted to the source), through a surface channel. The magnitude of this electron current is under control of the insulated gate. Past the p body region, the path of the electrons turns downward, vertically crossing the n^- epitaxial drift region and going into the n+ substrate drain region, the contact for which is on the bottom side of the power MOSFET die. From a MOSFET current control standpoint, the FET channel length, L in Figure 1a, is determined by the difference in the lateral extent of the p body diffusion and the n^+ source diffusion, with values of the order of L=1 μm typical for power MOSFETs. It is important to note that the actual on resistance, R_{on}, of the standard power MOSFET device is substantially higher than the channel resistance (specifically, the channel resistance plus twice the source resistance, as for a symmetrical planar MOSFET), due to the electron current path passing vertically through the n^- drift layer and the n^+ substrate thickness to reach the drain contact.

Comparison of Die Area Required for Deep-Submicron Planar Current Switching MOSFET to Achieve Given Value of R_{on} to Conventional Power MOSFET

The principal advantage of this conventional power MOSFET device structure, in addition to its ability to handle comparatively large drain voltages, is its convenient contact arrangement. The high-current drain contact covers the entire bottom of the die, while the high-current source contact covers most of the top of the die, sharing that surface with a smaller gate contact. This convenient die contact arrangement makes it easy to package the chip in a simple high current package. The principal disadvantage of the conventional power MOSFET structure is that even though the structure of source islands with channel borders shown in Figure 1a is packed into a dense 2-dimensional array covering the die surface, even with an aggressive 10^6 islands/cm² (10,000/mm²) array packing density, the potential amount of MOSFET periphery (width, W, of the surface channel per unit area, assuming W=20 μm/island), is only about W/A_{chip}=200 mm/mm² (reduced by ~10% for gate contact area). As a comparison, the planar horizontal geometry current switching MOSFET structure according to aspects of this invention gives W/A_{chip}=926 mm/mm² in a nominal 2λ=0.24μm feature size CMOS process (or about W/A_{chip}=850 mm/mm² including gate routing area), 4.63 times higher. Since for a given channel sheet conductance, the channel resistance is proportional to L/W, the other critical dimension for the power MOSFET is the channel length, L. As noted in Figure 1a, L=1.0 μm is typical for the channel length of a conventional power MOSFET. In comparison, the effective channel length in a 2λ=0.24μm feature size CMOS process is typically L_{eff}=0.19 μm or less. Hence for the same MOSFET periphery, the deep-submicron short-channel planar MOSFET devices used in aspects of this invention offer nominally 5.26 times lower channel resistance than a conventional power MOSFET. When this is combined with the fact that the periphery available in a given chip area is also 4.63 times higher, for a given chip size, the 2λ=0.24μm feature size CMOS process planar current switching MOSFETs

of aspects of this invention will have a channel resistance over 24 times less than that of a conventional power MOSFET.

The structure of the horizontal or planar geometry short channel current switching MOSFET is illustrated in Figure 1b. The basic device structure consists of a series of parallel n^+ stripes with poly silicide contacts, which represent the alternating source and drain electrodes, separated by poly silicide gate electrodes insulated from the silicon surface by a very thin (e.g., t_{ox}=5.8 nanometers) insulating layer which allows channel conduction to be controlled fully with very small gate voltage changes (ΔV_{gs}~2.5V). The electron path is essentially horizontal through the surface channel from the n^+ source to the n^+ drain electrodes. Typical dimensions in a 2λ=0.24μm feature size CMOS process are a nominal gate length of 2λ=0.24μm (L_{eff}=0.19 mm effective channel length), with source and drain contact widths of 7λ=0.84μm, for a total MOSFET pitch of 9λ=1.08μm (the reciprocal of which gives the W/A_{chip}=926 mm/mm^2 periphery to area ratio cited above). In fact, it is possible to fabricate substantially higher density MOSFETs in a such a λ=0.12μm CMOS process, with as low as ~6λ=0.72μm pitch, but in aspects of this invention it is desired to keep the total device resistance, including contacts and metal interconnects, as small as possible. Because the sheet resistance of the poly silicide source and drain contacts is relatively high (~4 Ω/square), it is important to minimize the distance the current passes laterally through the poly silicide contact before it reaches metal. As shown in Figure 1b, a 7λ=0.84μm source/drain (S/D) stripe width allows for a continuous chain of poly silicide to M1 (first level interconnect metal) via contacts to be placed down the center of these S/D stripes, making the poly silicide degradation of R_{on} negligible.

Comparison of Gate Drive Power Required for Planar Current Switching MOSFET to Achieve Given Value of R_{on} to that of Conventional Power MOSFET

To reiterate, the enormous (24x nominal) advantage in required silicon die area to achieve a given on resistance of the planar or horizontal geometry current switching MOSFET structure of aspects of this invention as compared to a conventional vertical power MOSFET structure comes about through the combination of the 4.63x greater FET periphery, W, that can be packed into a given area (due to the smaller feature size), and the 5.26x lower channel resistance for a given periphery (due to the shorter L_{eff}). This greatly reduced die size offers both a greatly reduced die cost and the opportunity for miniaturizing power conversion products. An additional benefit of this approach is the enormous reduction in gate drive power it affords. Ignoring parasitic contributions to gate capacitance, the charge, Q_g, furnished to the gate electrode will nominally equal the charge induced in the surface channel of the MOSFET. For an n-channel MOSFET with channel length, L, having a channel electron mobility of μ_e, the channel resistance, R_{ch}, at low drain voltages will be given as

$$R_{ch} = L^2/(\mu_e Q_g) \qquad \text{(for very low } V_{ds}\text{)} \qquad \text{Eq. 4}$$

Comparing the L=1.0 μm channel length of conventional vertical power MOSFETs with the L_{eff}=0.19 μm channel length of the planar devices of aspects of this invention means that, for the same μ_e, the gate charge to reach a given R_{ch} value will be 27.7 times smaller for the new planar current switching MOSFETs. Further, with a gate voltage swing, ΔV_{gs}, the ac gate drive power, P_{gd}, required to furnish this gate charge (i.e., to charge and discharge the gate capacitance , $C_{gs}+C_{gd}$) at a switching frequency, F_c, will be given by

$$P_{gd} = 1/2\,(C_{gs} + C_{gd})\Delta V_{gs}^2\, F_c = 1/2\ Q_g\ \Delta V_{gs}\, F_c \qquad \text{Eq. 5}$$

The magnitude of the gate voltage swing, ΔV_{gs}, required to transfer the gate charge, Q_g,= $(C_{gs}+C_{gd})\Delta V_{gs}$ is determined by the gate oxide thickness, t_{ox}. The gate capacitance of a MOSFET with channel length, L, and periphery, W, is given by

$$C_{gs} + C_{gd} = \varepsilon_o \varepsilon_r L\, W/t_{ox} \qquad \text{Eq. 6}$$

where ε_o=8.85x10^{-14} F/cm and ε_r=3.9 for an SiO_2 gate dielectric. From Eqs. 4-6, the channel resistance of the MOSFET will be given by

$$R_{ch} = L^2/(\mu_e Q_g) = L\, t_{ox}/(\mu_e\, \varepsilon_o\, \varepsilon_r\, W\, \Delta V_{gs}) \qquad \text{Eq. 7}$$

This means that the gate voltage above threshold, ΔV_{gs}, required to reduce the channel resistance to a given R_{ch} value, as given by

$$\Delta V_{gs} = L\, t_{ox}/(\mu_e\, \varepsilon_o\, \varepsilon_r\, W\, R_{ch}) \qquad \text{Eq. 8}$$

is proportional to the oxide thickness, t_{ox}. Substituting Eq. 8 into Eq. 5 shows that the amount of ac gate drive power, P_{gd}, required to switch the MOSFET to a channel resistance, R_{ch}, will be given by

$$P_{gd} = 1/2\, F_c\, L3\, t_{ox}/(\mu_e^2\, R_{ch}^2\, \varepsilon_o\, \varepsilon_r\, W) \qquad \text{Eq. 9}$$

This is an important result which indicates that a given switching frequency, F_c, for MOSFETs with the same W/L ratio and channel mobility, in addition to the factor of L^2 that comes from the required gate charge (Eq. 5), the gate drive power expression has an additional factor of t_{ox} in it. Hence, if we compare the planar geometry current switching MOSFET of aspects of this invention with L=L_{eff}=0.19 μm and t_{ox}=5.8 nm with a typical vertical geometry power MOSFET having L=1.0 μm and t_{ox}=100 nm, we see that in addition to the L^2 advantage of 27.7x, we have a t_{ox} advantage of 17.24x, which means that the ac gate drive power is reduced by an factor of 478x by going from a conventional vertical power MOSFET to the deep-submicron planar MOSFET structure of aspects of this invention. This amazing (nearly 500x) reduction in gate drive power lets this new planar short channel

current switching MOSFET be operated at much higher switching rates without seriously compromising power efficiency, which in turn allows for greatly reducing the size of switching power converters, etc., because of the reduced sizes of the capacitors and magnetic elements.

It should be noted that while Eq. 5 is exact, due to higher vertical electric fields at the gate oxide interface, the channel mobilities, μ_e, in deep-submicron MOSFETs will be somewhat smaller than those for power MOSFETs. On the other hand, while the total MOSFET device "on" resistance, $R_{on(f)}$, of the planar geometry MOSFETs of aspects of this invention (Figure 1b) are given from the channel resistance, R_{ch}, and the source and drain contact resistances, R_s and R_d, (normally $R_s \cong R_d$ due to symmetry) by

$$R_{on}(f) = R_{ch} + R_s + R_d \cong R_{ch} + 2R_s \quad \text{(for planar MOSFETs)} \qquad \text{Eq. 10}$$

for the unsymmetrical vertical geometry power MOSFET structure of Figure 1a, there is a substantial additional drain resistance component due to the n^- drift layer in Figure 1a that makes $R_{on(f)}$ substantially greater than R_{ch} + 2 R_s. Hence a substantially lower R_{ch} value must be achieved in the vertical power MOSFET in order to achieve the same total device resistance, $R_{on(f)}$, . Additionally, while Eq. 6 is a good approximation for the gate capacitance in the planar MOSFET structure, the large gate area over the n^- drain region (see Figure 1a) makes the actual gate capacitance at low V_{ds} for the conventional vertical power MOSFET structure much larger than indicated by Eq. 6. Hence the nearly 500x gate drive power advantage of the planar geometry short channel MOSFETs of aspects of this invention over conventional vertical power MOSFETs should at least be reasonably accurate, and probably understates the advantage.

<u>Capability of Some Embodiments of Invention to Realize Very High-Speed, Ultra-Low Q_d Body Diode</u>

The capability of a CMOS integrated circuit fabrication process to make, in addition to the n-channel MOSFETs discussed above, isolated p-channel MOSFETs (as shown in Figure 1b), can also be exploited to advantage in designing high current switching planar MOSFETs as well. Figure 2a shows the equivalent circuit of a conventional vertical power MOSFET. Note that, in parallel to the n-channel MOSFET device, there is a robust p-n junction body diode which is capable of passing high levels of current if the drain is made more negative than the source by $V_{fp\text{-}n}$=1.0V or so. While in some switching circuit applications where the synchronous rectifier switch timing is not precisely matched to the secondary current timing, the "freewheeling" currents can be handled by the p-n body diode. Unfortunately, the relatively high forward voltage drop of the body diode will degrade the power efficiency of low voltage converters substantially if the duration of the freewheeling currents is a significant fraction of the total switching cycle. In addition to the high p-n body diode forward voltage drop, they also have serious charge storage problems (large Q_d values) that limit usable switching frequencies. In the short-channel

CMOS-implemented planar current switching MOSFET device of aspects of this invention, it is possible to use the p-channel device to implement a relatively low forward voltage drop "diode" having virtually no charge storage (near-zero Q_d). The optional circuit for adding this "body diode" capability to an n-channel device is illustrate in the equivalent circuit of Figure 2b. This "body diode" function is emulated by an active diode-connected p-channel MOSFET (i.e., the gate is connected to the drain). When the drain electrode becomes more negative than the source by a voltage equal to the gate threshold voltage, V_{tp}, the p-channel device will begin strong conduction. Since a typical value for this gate threshold voltage is V_{tp}=-0.28V, the V_{fpch} forward conduction voltage drop can be much lower than for a p-n junction body diode. When the drain terminal is more positive than the source, as when the n-channel device is conducting normally, the p-channel device conduction is cut off. There is negligible charge storage associated with the transient transition of this diode-connected p-channel MOSFET "body diode" from strong "forward" conduction to "reverse bias" cutoff (principally the small $C_{gs}+C_{gd}$ of the p-channel MOSFET plus some n-well to p-substrate capacitance).

As noted in Figure 2b, this "body diode" function can equally well be implemented with an n-channel MOSFET whose gate is connected to its source. When the drain electrode becomes more negative than the source by a voltage equal to the gate threshold voltage, V_{tn}, the n-channel device will begin strong conduction. This is because when the drain of the symmetrical n-channel MOSFET is taken more negative than the source, the source behaves like the drain and visa versa, so the gate is now connected to the (effective) drain, which is the usual configuration for connecting a MOSFET as an active diode. Note that this also means that if we constrain the gate voltage of the "OFF" large n-channel current switching MOSFET to go no more negative than its source [$(V_{gs})_{off}$=0], then this n-channel current switching MOSFET will act, by itself, as a "body diode" with no additional structures necessary.

Interconnect/Packaging Approach for Ultra-Low Resistance Connection of Deep-Submicron Planar Current Switching MOSFET Die to Circuits

While the electrical characteristics of the planar geometry deep-submicron current switching MOSFET structure of aspects of this invention represent an enormous improvement over conventional power MOSFET devices in terms of much smaller die sizes, higher switching speeds and remarkably lower gate drive requirements to achieve a given value of on resistance, R_{on}, it requires a carefully designed interconnect and packaging approach to realize the die-level performance in actual circuit application. The basic approach to achieving this is illustrated in Figure 3, which shows a cross-sectional view of the planar (horizontal) geometry MOSFET structure with its on-chip interconnects, solder ball array die to package mating, and high-current low-resistance package. Note that in order to maintain visibility of the on-chip interconnect structure, the vertical dimensions of the thicker elements such as silicon die thickness, die to package (and solder ball) thickness, and thickness of package copper layers have been reduced in Figure 3.

The basic interconnect/packaging approach is to make use of an area array of a large number of source (S) and drain (D) pads, in addition to a few gate (G) pads, covering the full area of the planar geometry current switching MOSFET die. In a preferred embodiment of this invention, illustrated in Figure 3, solder balls are formed on each of these pads for flip-chip mating to the mirror-image pad array on the high-current package. As the density of the pad array is increased, or pitch between the solder balls decreased, the height of the solder balls is generally proportionally decreased. Hence as the center-to-center pitch, P_{sb}, of the solder balls is reduced, the number of balls, N_{sb}, on a chip of area, A_{chip},

$$N_{sb} = A_{chip}/P_{sb}^2 \qquad \text{Eq. 11}$$

increases as $1/P_{sb}^2$, while the resistance per ball, R_{psb}, increases as $1/P_{sb}$ (since the ball height and diameter go as P_{sb}, the height to area ratio goes as $P_{sb}/P_{sb}^2=1/P_{sb}$) , so the combined solder ball resistance varies as

$$R_{sb} = 4\ R_{psb}/N_{sb} \ \propto 1/P_{sb} \qquad \text{Eq. 12}$$

(The factor of 4 in Eq. 12 comes from assuming that if there are N_{sb} total solder balls on the die, approximately 50% will be used for source contacts and the other 50% for drain contacts, accounting for a factor of 2, while the R_{on} will be degraded as the sum of the source and drain contributions, accounting for the other factor of 2.) What Eq. 12 illustrates is that the total pad contact resistance can be reduced by making the solder ball pitch as small as possible (the ball array density as large as possible). The pitch effect is even stronger in the reduction of the metal spreading resistance, which tends to fall nearly as $1/N_{sb}$ or $1/P_{sb}^2$. Hence the use of a high-density array of as many solder bumps as possible covering the surface of the die reduces both the solder bump and the metallization (on-chip and package) contributions to the "on" resistance of the packaged planar current switching MOSFET devices. While typical commercial flip-chip solder bump array pitches of P_{sb}=250μm are adequate for useful performance, the total metallization plus ball resistance can be several times the intrinsic MOSFET device resistance (Eq. 10) (or somewhat less if a copper interconnect metallization technology is used on the chip). By using the highest commercially available solder bump array density, P_{sb}=100μm, the total (chip plus package) metallization plus solder ball resistance may be reduced by about a factor of three, to make it comparable with the intrinsic MOSFET device resistance (e.g. ~75μΩ for a 4mm x 4mm die with a typical aluminum metallization technology).

<u>On-Chip</u> <u>Interconnects</u>

In the cross-section drawing of Figure 3, there are 5 levels of on-chip metallization illustrated, typical for a current 2λ=0.24μm feature size commercial CMOS IC foundry process. In the cross section drawing of Figure 3, and in the associated mask layer sequence layout drawings in Figures 4A – 4B and 5A – 5B, the use of the various chip metallization layers is shown. The chip layout actually begins

with the shallow trench isolation of the p-well in which the n-channel MOSFETs are defined. While the shallow trench isolation is not illustrated in Figures 4A – 4B, it would occupy the 3 μm space between the 25μm high rows of MOSFET channels, somewhat wider than the M1 and M2 gate (G) busses. The upper left layout (Figure 4A) shows the 7λ=0.84μm wide by 25μm long poly silicide source/drain (S/D) stripes, plus the row of 2λ=0.24μm square via cuts which connect them to the M1 stripes above them. These M1 stripes, plus their vias up to M2 are shown at the upper right (Figure 4B). The structure up through M1 is also illustrated in the cross sections of Figures 1b and 3. As seen at the lower left (Figure 4C), M2 is dedicated mainly to horizontal S and D busses, plus the smaller horizontal gate bus (which is in parallel to its counterpart on M1). M3, as seen at the lower right (Figure 4D) (and reproduced at the upper left Figure 5A) is a dedicated S (source) plane, with a substantial number of drain (D) feedthrus (and a much smaller number of gate (G) feedthrus) penetrating it. Similarly, as seen at the upper right in Figure 5B, M4 is a dedicated D plane, with S and G feedthru patches to reach up to the S and D contact "checkerboard" (and gate contact "grid" in between) that makes up M5. The lower left drawing in Figure 5C shows a portion a source and a drain contact pad and the vertical M5 gate "grid" stripe between them (these tie all of the horizontal M1/M2 G busses together into a single gate connection, to which are assigned four M5 gate pads). The total chip layout at the lower right illustrates a 4 mm x 4 mm chip carrying 256 solder ball pads on a P_{sb}=250μm pitch. As illustrated in the cross-sectional drawing of Figure 3, the actual solder ball base is a 125μm diameter circle, centered on each of the square M5 contact pads, that is defined by a hole in the oxide protection coating ("scratch mask").

Package Interconnects

Because of the concentration of current, and requirement for carrying the current laterally over substantial (many mm) distances, the metallization thicknesses in the package must be quite substantial (e.g., hundreds of microns of copper in the thicker layers). Figure 6A and Figure 6B show respective cross-sectional and plan views of an example of the layout of a package with planar bottom source and drain contacts (e.g., suitable for surface mounting on a circuit board). In the example illustrated, the base substrate is a 500μm (20 mil) thick copper-invar-copper (to provide a coefficient of thermal expansion [CTE] reasonably closely matched to that of the silicon die). While initially this base substrate is continuous, during processing it is sawn or etched through for electrical isolation, with the major area chosen as the source (S) package contact, while a smaller end region (the right end in Figures 6A and 6B) is the drain (D) package contact. The lateral current flow from the drain solder balls from the die to the drain contact end is through a thick copper layer (e.g., 250mm [20 mils] thick plated copper in Figure 6B). The lateral current from the source solder balls to the opposite, source contact, end of the package is through the 20 mil thick copper-invar-copper substrate, but the current reaches this substrate by passing through the 10 mil thick Cu drain plane via an array of isolated copper "studs" or "plugs" penetrating the plane.

While it would be advantageous to make the center-to-center pitch of these studs as fine as possible (e.g., the same pitch as the solder bumps on the die would be ideal), due to the 10 mil thickness of the copper layer through which they pass this is impractically difficult. In typical circuit plating processes, the aspect ratio (metal layer thickness divided by minimum horizontal feature size) is typically kept to 1:1 or less. (Higher aspect ratios can be fabricated using more exotic processes, but their higher costs would make them economically unsuitable for most applications at present.) In the package structure illustrated in Figures 6A and 6B, the smallest feature to be defined in the 10 mil thick plated copper layer would be the narrow isolating gap ("moat") surrounding each source plug (via) penetrating the layer. The plug itself is of reasonable dimension to carry S current vertically with low resistance, while the outer rims of the isolation moats do not get too close together or they will impede the lateral flow of drain current through this 10 mil thick plated copper drain plane. Hence, keeping the aspect ratio near 1:1, with a 10 mil thick drain plane, the nearest center-to-center stud pitch (diagonal in Figure 6A) cannot be much less than 25-30 mils. It is advantageous in the layout to make the horizontal stud (via plug) pitch an even integer multiple of the die solder ball pitch, so for the P_{sb}=250μm (~10 mil) ball pitch, a 1.000 mm (~40 mil) horizontal stud pitch (0.7071mm [27.84 mils] minimum [diagonal] pitch) is chosen in Figure 6A.

While the drain plane lies directly under the drain solder balls (unless the via stud isolating moats are too large, causing some of the drain solder ball contacts to fall "off the edge" of the drain plane metal onto the moat), this is not the case for the source solder ball contacts, only a small fraction of which fall on studs. The connection of the source solder balls to the studs (via plugs) utilizes an additional layer or two of copper that is capable of being more finely patterned than the drain plane (and which hence are much thinner). This source plane metallization (seen more easily in the cross-section of Figure 3 than in that of Figure 6B) could have one or two layers of fineline copper about 10μm in thickness (about 1/25th of the thickness of the 10 mil thick drain plane). Creating these higher density (smaller feature size) multi-layer interconnects requires a reasonably flat surface to start with, which means that the moats are filled around the plugs with a suitable dielectric material and planarize the dielectric and copper surface before the copper/BCB (or other suitable multilayer dielectric material) interconnect layer(s) are applied. While the moat diameter shown in Figure 6A would allow drain contacting and the source plane to be created in one metal layer, in most cases it would be advantageous to have at least two fineline copper interconnect layers, both to facilitate getting the drain solder ball contacts down to the 10 mil copper drain plane and to reduce the spreading resistance from the source studs out to the majority of the source solder balls that do not sit on studs, as well as to facilitate making contact to the gate pads without significantly degrading this source plane resistance.

Alternative Wafer-Level Additive Copper/Polymer Packaging Approach

As described in the following section (Table 1), the contribution of metal resistance, both on-chip and package, to R_{on} can be reduced by increasing the density of solder ball contacts between the die and the package. In the packaging approach illustrated in Figures 3 and 6A and 6B, the solder balls ("bumps") are fabricated directly on the completed IC wafer using standard commercial bumping processes (it is also possible to bump individual die, but wafer bumping is cheaper). While 100μm solder bump pitches in area arrays are commercially available, the technology is not as well developed as the more common 250μm pitch, and the reliability is problematical where significant package to silicon wafer CTE differences may exist. Also, with a 100μm bump pitch, the need for one or two layers of "fineline" additive interconnect metal (as illustrated in Figures 3 and 6A and 6B) to the high-current package structure is desired in some aspects. This adds to package complexity and makes finding suitable commercial sources for the package more difficult.

The alternative packaging approach illustrated in Figure 7 achieves the very low R_{on} of the 100μm solder ball approach (or exceeds its performance) while reducing the demands on both the solder bump mating technology and the package. The concept is to fabricate the one or two (as illustrated in Figure 7) "fineline" metal layers (e.g., 5μm to 20μm of copper) with polymer (e.g., BCB or polyimide) interlayer dielectric directly on the completed IC wafer in a full-wafer process. Applying the additive copper/polymer interconnects directly to the "completed" IC wafer (i.e., the wafer has passed through all of the normal fabrication steps of the CMOS IC foundry) will in general be less expensive and more practical than adding them on the package side. It is more practical because this copper/polymer technology is not generally available at package vendors. It is less expensive because of the fact that die area is smaller than that of the package; hence a smaller area of material is subjected to the cost of the copper/polymer processing when it is placed directly on the die. (In the case of very low yields of "good" die on the IC wafers, the cost of putting the "fineline" copper/polymer interconnects directly on the IC wafers could exceed that of applying them to the packages, but such low yields of good die would not be expected for mature CMOS foundry processes.)

In addition to being more practical and lower cost, applying the additive copper/polymer interconnects directly to the "completed" IC wafer offers the advantage that the density of interconnections between the normal CMOS on-chip metallization and the much thicker "fineline" copper layers is not limited by any solder bump or other joining technology, but only by the via density and metal linewidths available in the first layer of copper/polymer interconnects. The interconnect densities practical between the IC chips and an additive copper/polymer are not only much higher than solder bump densities, but there is no reliability penalty associated with going to very high via densities on a chip like there is in joining technologies such as solder bumps. In the approach of Figure 7, there is very little R_{on} penalty associated with using relatively coarse solder bump (or

solder stripe, etc.) pitches because the of the low sheet resistance of the additive copper layers. Hence, the solder contacts may go directly from the die (with the copper/polymer "fineline" layers on it) to very thick metal package structures having very coarse feature sizes (such as going to an interdigitated thick (e.g., >20mils) copper-invar-copper package or some form of laminate package).

Alternative Vertical Laminate Package Approach

The package geometries illustrated in Figures 3 and 6A and 6B are horizontal, in that layers of metal conductors carrying the high MOSFET source and drain currents lay parallel to the surface of the MOSFET die. In this geometry, via structures carry current between the different patterned layers of package metallization. These vias (more specifically, the spreading resistance of getting currents into and out of the inter-layer via areas) represent a significant contribution to the overall package metal resistance, as well as a source of concern for package reliability. Also, the fact that the vertical thickness of the metal layers is limited by practical fabrication considerations that limit the layer thicknesses to be of the order of the horizontal feature sizes provides a further limitation on package resistance for the horizontal package geometry.

These limitations can be overcome and extremely low package resistances achieved by going to a vertical laminate package geometry, as illustrated for the case of the monolithically-integrated gate drive amplifier (Figure 8) in Figure 9A and 9B. In this structure, the high source and drain currents are carried in vertical metal layers (that is, perpendicular to the surface of the current switch MOSFET die). Their (horizontal) thickness is limited by the feature size of the die contacts (e.g., solder bump pitch), but their vertical extent is unlimited, so that extremely low package metal resistance levels can be achieved. Note that ordinarily, the separation of the high current paths is achieved in the vertical laminate package by sweeping, for example, the layers contacting the source rows of solder balls in one direction and those contacting the drain layers in the opposite direction (e.g., in the illustration at the bottom (Figure 9B), the source layers might be swept in the direction into the page, and the drain layers out of the page). Alternatively, rows may be dedicated to other purposes such as low inductance V_{dd} connections and they can be taken out of the package bottom, in addition to the opposing sides (or either the source or drain connection could be taken out of the package bottom if desired). Note that while the attachment of this vertical laminate package directly to solder balls on die metallization pads is shown in Figure 9B, this package configuration can also be very advantageously used with a die with the additive "fineline" thick copper interconnects added as illustrated in Figure 7. When the additional copper/polymer interconnect layers are added to the die, the pitch of the solder contacts to the package may be greatly increased without significantly degrading R_{on}. This means that fewer layers of laminate are needed for the package, making it easier to match the laminate layer pitch to the solder contact pitch, and potentially making practical the use of materials like copper-invar-copper (CIC) for the metal layers in the laminate stack for improved CTE match to the silicon die, which would offer the

potential for improved reliability. Note that while the use of CIC in the laminate package stack would alleviate CTE mismatch in the plane of the metal layers, there could still be CTE mismatch in the perpendicular direction due to the CTE of the organic dielectric layers in the stack. If, however, the organic dielectric interlayers are pulled back from the solder interface to the die (further than the pullback illustrated at the bottom Figure 9B), then this perpendicular CTE mismatch may be compensated for by a small amount of bending in the laminate metal layers.

Calculated Performance for Packaged Planar Current Switching MOSFET Devices

It is of value to calculate the intrinsic device, on-chip metal, and package metal contributions to the on resistance, R_{on}, as well as other critical performance parameters that would be expected for a planar current switching MOSFET device of the type described in aspects of this invention. Since, as noted in Eq. 12, the metal interconnect resistance decreases as the density of the solder ball interconnects is increased, two cases will be presented; one assuming 125μm balls on a 250μm pitch (standard commercial area array solder ball practice), and the other assuming 50μm balls on a 100μm pitch (highest area array solder ball density that is commercially available at present). A silicon die area of 4mm x 4mm was assumed for the planar current switching MOSFET device, so that the total number of solder balls was 256 for the 250μm pitch or 1600 for the 100μm pitch case. Using design rules for a commercial $2\lambda=0.24\mu m/L_{eff}=0.19\mu m$ CMOS process, with a layout of the type illustrated in Figures 3-5D, a total FET width of 13.5 meters is achievable in the 4mm x 4mm chip size. This process has a $t_{ox}=5.8$ nm gate oxide thickness which gives an N-channel resistance, R_{ch} (Eq. 7), at $V_{gs}=+2.5V$ of 43μΩ for the $L_{eff}=0.19mm/W=13.5m$ MOSFET of only 43μΩ. When the $R_s=R_d=14.1\mu\Omega$ source and drain resistances are added to R_{ch} (as per Eq. 10), the intrinsic device on resistance is calculated to be only $(R_{on})_{dev}=71.1mW$.

The CMOS process analyzed has a 5-layer aluminum on-chip metallization system, with metal layers M1-M4 having a resistance of 0.088Ω/sq and M5 having 0.044Ω/sq, while the S/D silicide has 4.0Ω/square. The via cut resistances are 7.5Ω/cut between the S/D silicide and M1, and 5Ω/cut between M1 and M2 or between other metal layers. While a 7.5Ω/cut S/D silicide to M1 metal layer resistance may sound serious, for a W=13.5 meter MOSFET width, there are 13.5 million of these via cuts in parallel in both the source and drain paths to share the current, so the addition to R_{on} is only 1.11μΩ. This parallelism applies to the other metal resistance contributions, as a consequence of a chip interconnect layout (Figures 4 and 5) that is well thought out to minimize metal resistance. A resistance build-up analysis of the various spreading resistances in the on-chip metal planes and the inter-layer via cut resistances gives a calculated on-chip metal resistance of 54.6μΩ in the source lead and 55.9μΩ in the drain lead (110.5μΩ total S+D) for the 250μm solder bump pitch, which drops to 14.1μΩ in the source lead and 15.5μΩ in the drain lead (29.6μΩ total S+D) for the finer 100μm solder bump pitch.

Similarly, the package metal resistance is also a function, though slightly less dramatic, of the solder bump pitch in the flip-chip area array interconnects between the planar current switching MOSFET die and its package. A resistance build-up analysis of the various spreading resistances in the package metal planes and through-layer "plug" resistances gives a calculated package metal resistance of 54.6μΩ in the source path and 55.9μΩ in the drain path (110.5μΩ total S+D) for the 250μm solder bump pitch, which drops to 33.6μΩ in the source path and 46.0μΩ in the drain path (79.7μΩ total S+D) for the finer 100μm solder bump pitch. Table 1 summarizes the contributions to the packaged device Ron (total source + drain) of the MOSFET device, the on-chip metallization, and the package metallization (including solder balls) for the "standard" (250μm) and "high-density" (100μm) chip-to-package solder ball array pitches.

	Solder Ball Pitch Cases	
	Standard P_{sb}=250 μm	**High-Density** P_{sb}=100 μm
Silicon/Transistor (V_{gs}=+2.5V):	71.1 μΩ	71.1 μΩ
On-Chip Metallization:	110.5 μΩ	29.6 μΩ
Package Metal:	103.2 μΩ	79.7 μΩ
Total Resistance (Si+Metal+Package):	**284.8** μΩ	180.4 μΩ

Table 1. Calculated contributions to R_{on} for planar L_{eff}=0.19μm current switching MOSFET ($C_{gs}+C_{gd}$=20nF for W=13.5m, 4mm x 4mm die).

Note in Table 1 that even with the high-density solder ball pitch, the largest contribution to R_{on} is the metallization, not the MOSFET device itself, and that the largest contribution to the R_{on} resistance is from the package metallization. This is a result of the fact that we have assumed a convenient planar, surface-mountable package configuration (Figures 6A and 6B). It would be possible to substantially reduce the package metal resistance by reducing the horizontal distance through which the source/drain current must pass between the die and the package S/D contacts. One package configuration which would accomplish this would be a vertical package geometry with the source lead on the bottom (as it is under the chip in Figure 6B), but with the drain lead on the top, surrounding (and probably covering) the planar MOSFET die. This could be accomplished, for example, by bringing the 10 μm thick plated copper drain plane up to the surface around the die, and then using either a plated copper wall or preform to bring the contact surface above the height of the die. It would be possible to use a cover lid on this drain contact ring, or leave the back of the die exposed (with suitable underfill passivation). This configuration would reduce both the total package area and its

contribution to R_{on} substantially, and could represent a convenient form factor for some applications.

It should be noted that the flip-chip die underfill noted above would probably be utilized in either the flat, surface-mount version of the package shown in Figures 6A and 6B, or in a vertical package geometry of the type just discussed. One reason for this is that underfill is an effective means of enhancing solder ball reliability in the face of differential thermal expansion between package and silicon die. Another is that the constraint provided by the underfill could be of substantial value in reducing lifetime degradation due to electromigration in the solder bump metal. The planar MOSFET die in this example should be able to switch currents of 200 amperes, even though the die is only 4mm x 4mm in size. This pushes, however, the conventional operational current density of solder ball contacts to die for high reliability. This is not viewed as a serious concern, however, both because the constraint of the underfill should minimize the problem, and because of the way the solder balls are used in this application. In usual flip-chip reliability analyses, it is assumed that the failure of any single solder ball represents a functional failure of the part. In this planar current switching MOSFET structure, there is massive parallelism between the current-carrying (S/D) solder balls. For example, for the high-density (P_{sb}=100 μm ball pitch) case, there will be a total of 1600 solder balls, or 800 balls in parallel in the source path and 796 balls in parallel in the drain path (assuming 4 balls for gate leads). The complete failure of even 10% or 20% of the solder balls mating the die to the package would make a barely-perceptible change in the R_{on} of the packaged device. (This is because the total S+D solder ball resistance contribution to the 180.4 μΩ R_{on} value is only 8.4 μΩ, and while failed balls would also locally increase the metal plane spreading resistances, the effect of even 20% randomly-distributed ball failures is very small.) The favorable statistics in this application where 10% to 20% ball failures have no significant effect, as compared to the usual "one ball failure is death" condition allows us to push to higher than normal current densities in the solder balls. Of course, if solder ball electromigration remains an issue in some applications, solder ball metal compositions more resistant to electromigration effects at the desired operating temperature can be utilized. Note that as discussed in the previous section, the alternative packaging approach of fabricating copper/polymer "fineline" interconnect layer(s) directly on the completed CMOS wafers has the advantage of achieving R_{on} performance at least as good as shown for 100μm solder balls in Table 1, while using a relatively coarse feature size joining technology which should offer reliability advantages over fine-pitch solder balls.

It should be noted that whether the planar package configuration of Figures 6A and 6B (R_{on}=180.4 μΩ) or the vertical package geometry (R_{on}=125 to 150 μΩ estimated) is used, the packaged device resistances are almost unbelievably small for such a small device (4mm x 4mm die, 12mm x 7mm planar package, or about 6mm x 8mm for a vertical package with the same die). Even at a 200 amp drain current, R_{on}=150 μΩ represents only a V_{ds}=30 mV voltage drop.

Gate Drive Requirements and Optional Device Features

A dramatic difference between the horizontal or planar geometry deep-submicron channel length current switching MOSFET structure of aspects of this invention and conventional vertical geometry power MOSFETs is in their gate drive requirements. In the example cited above, the total calculated gate capacitance is only $C_{gs}+C_{gd}$=20 nF (Eq. 6, with ε_r=3.90, L=0.24µm, W=13.5m and tox=5.8nm gives $C_{gs}+C_{gd}$=19.28nF). This is far (1 to 2 orders of magnitude) less than the gate capacitance of conventional vertical power MOSFETs having a comparable R_{on} values. (Actually, many conventional power MOSFETs connected in parallel would be required to reach this Ron level; it is the total $C_{gs}+C_{gd}$ value for the paralleled power MOSFETs that is compared to the $C_{gs}+C_{gd}$=20 nF value of the planar switching MOSFET of aspects of this invention.) Also, while conventional power MOSFETs require V_{gs}=10 V or more gate voltages to reach low R_{on}, with aspects of this invention the values in Table 1 are reached with only a V_{gs}=2.5 V gate drive voltage. As discussed previously, the combination of the lower value of $C_{gs}+C_{gd}$ and the lower V_{gs} gate drive voltage requirement drastically lowers the (Eq. 5) $P_{gd} = 1/2 (C_{gs} + C_{gd}) \Delta V_{gs}^2 F_C$ gate drive power requirements for the planar short-channel current switching MOSFET of aspects of this invention (by nearly a factor of 500 over conventional power MOSFETs).

One of the implications of this enormous reduction in ac gate drive power is that it becomes practical to sharply increase the switching frequency, F_C, without serious efficiency loss due. This makes it possible to reduce the size and weight of the capacitive and magnetic energy storage devices in a power converter circuit, to allow, for example, very small on-board switching power converters to be realized. For example, an V_{out}=1.2V switching converter having a maximum output current of 200 amperes (240 watts peak output) could be fabricated with two of these planar geometry current-switching MOSFETs, which would have, even at a very high F_C=1 MHz switching rate a total gate drive power of only P_{gd} =0.125 watts for the two synchronous rectifier switches, or 0.052% of the peak output power. This means that it would be quite practical to increase switching frequencies up into the many tens of megahertz range before gate drive power became a serious efficiency concern, which would allow for remarkable miniaturization of power converters.

The low gate drive power requirements, along with the fact that the planar geometry deep-submicron current switching MOSFET devices are conveniently (and inexpensively) fabricated using a standard deep-submicron CMOS foundry process, suggests a very attractive option: the inclusion of the gate driver amplifier on the same chip with the switching MOSFET. With conventional power MOSFETs, furnishing clean ("square-wave") gate drive voltages is a major problem, even at switching frequencies of the order of F_C=100KHz. While the planar geometry deep-submicron current switching MOSFET devices have low $C_{gs}+C_{gd}$=20 nF gate capacitances and are capable of operation at >10MHz switching frequencies at low gate drive powers, for clean, efficient square-wave gate voltages the pulsed gate

currents will be substantial. For example, if it is desired to keep the gate voltage risetimes and falltimes to less than 2.5% of the switching period at F_C=10MHz, the voltage risetimes must be under $t_r=t_f$=2.5ns. With ΔV_{gs}=2.5V and $C_{gs}+C_{gd}$=20nF, the gate drive current will pulse to $i_g=(C_{gs}+C_{gd})(\Delta V_{gs}/t_r)=\pm 20$ ampere levels in each MOSFET during the rise and fall intervals. The distributed inductance/characteristic impedance of usual on-board interconnects virtually precludes furnishing gate drive signals of this quality in a practical multi-package on board environment.

These gate drive signal limitations of conventional packaging can be overcome in the case of the planar geometry deep-submicron current switching MOSFET devices of aspects of this invention by placing the gate driver amplifier on the same silicon chip as the MOSFET, as illustrated in Figure 8. The gate driver amplifier would consist of a short chain of CMOS inverters (e.g., 2 to 4 stages typically; Figure 8 shows a 2-stage gate driver) between the gate input to the package/die and the actual MOSFET gates. In order to minimize ac gate current distribution problems, it would probably prove useful to distribute the last (largest) stage of the gate amplifier chain in sections around the chip. The sizing of the p- and n-channel MOSFET devices in the CMOS driver inverters can be estimated from the device characteristics and the desired gate drive currents. Consider a 2-stage CMOS inverter driver for the 200 ampere current switching MOSFET example, as shown in Figure 8. The saturated drain current for the L_{eff}=0.19μm n-channel MOSFETs in the 2λ=0.24μm feature size commercial CMOS foundry process is I_{dss}/W=0.6ma/μm with an $R_{on}W$=960Ωμm "on" resistance. The p-channel devices are about half as good (half the I_{dss}/W and roughly twice the $R_{on}W$), so for balanced current drive the p-channel MOSFETs are scaled about twice as wide as the n-channel devices. For convenience, the sizing (width, W) of only the n-channel devices will be cited, with the understanding that, as shown in Figure 8, the matching p-channel pull-up devices will be twice as wide. For a desired gate drive current pulse of 20 amperes into the W=13.5 meter, 200 amp current switching FET, a second-stage driver MOSFET width of W_{d2}=50mm (I_{dss}=30 amps) would more than suffice. Its R_{on}=0.0192Ω on resistance would give an $t_{rc}=R_{on}(C_{gs}+C_{gd})$=0.384ns time constant with the $(C_{gs}+C_{gd})$=20nF gate capacitance, which would give excellent gate voltage settling. The input gate capacitance, C_{in2}, of this W_{d2}=50mm driver output stage would be about 75pF for the n-channel device and 150pf for the (2x wider) p-channel MOSFET, or C_{in2}=225pF total. To drive this 225pF capacitance over its ΔV_{gs}=2.5V range in Δt_r=1ns would require $I_{in2}=C_{in2}\Delta V_{gs}/\Delta t_r$=563ma gate drive current pulses, which require that the prior first-stage driver have an n-channel MOSFET width of about W_{d1}=1.0mm (I_{dss}=600ma). The input capacitance for this first driver stage will be about 1.5pF for the n-channel, and 3pF for the p-channel MOSFETs, or 4.5pF total gate input capacitance for the chip. Since a 4.5pF gate driver input capacitance is very easy to drive with very fast edge rates with typical Z_o=50Ω characteristic impedance circuit board interconnects, the two-stage driver is more than adequate.

The inclusion of the on-chip gate driver amplifier allows the gate input of this 200 amp planar current switching MOSFET chip to be driven with remarkable timing precision with nothing more than conventional digital logic signals and circuit board interconnects. From a terminal count standpoint, it adds only two package connections; the V_{dd}=+2.5Vdc and V_{ss}=ground driver amplifier power inputs. While it would be possible, in principle, in some applications to tie the input stage amplifier V_{ss} power lead to the source lead of the current switching MOSFET, in many cases this could lead to feedback coupling problems/potential for oscillations on transitions, so a separate input stage V_{ss} ground lead is preferred. On the other hand, the high peak gate current spikes into the switching demand a very low impedance (particularly inductance) connection between the driver output stage and the switching MOSFET gate, most easily accomplished if we tie the driver V_{ss} power lead to the source lead of the current switching MOSFET. A side benefit to tying the V_{ss} lead of the amplifier driver (output) stage to the source of the switching MOSFET is that it automatically achieves the "body diode" of Figure 2B. When the input in Figure 8 is taken "LOW" ($\approx V_{ss}$) to turn off the current switching MOSFET, its gate will essentially tied its source through the "ON" W_{d2n}=50μm driver MOSFET. In this state, as noted in Figure 2B, the W_n=13,500μm current switching MOSFET will begin to conduct any time its drain voltage becomes more negative than its source by more than its gate threshold voltage, V_{tn}. While connecting the source of the W_{d2n}=50μm n-channel driver MOSFET directly to the source of the output current switch MOSFET solves the problem for handling the large (≈20 ampere) negative gate current peaks, the equally large positive gate current spikes out of the W_{d2p}=100μm p-channel driver MOSFET must also be dealt with. In the gate driver amplifier design in Figure 8, a large (>20nF) bypass capacitor is included between V_{dd} and the source of the current switching MOSFET. In the absence if this bypass capacitor, the full magnitude of the positive gate current spikes would have to be furnished through the V_{dd}=+2.5V gate driver amplifier supply, which would require an extremely low ac impedance (particularly inductance) to the V_{dd} lead in order to avoid "voltage starvation" during positive gate current transients which would compromise the switching process. The inclusion of the on-chip bypass capacitor as an extremely low inductance source of the charge required to charge the gate capacitance of the large current switching MOSFET makes an ultra-low inductance V_{dd} connection to the chip unnecessary. It has, however, some chip area/cost penalty. The increase in chip area due to the gate driver amplifier itself is minimal, adding a total of only $W_{d(n+p)}$=153mm (W_{d2}=50mm + W_{d1}=1.0mm, or 51mm of n-channel MOSFET width, plus twice that, or W_{d1p}+W_{d2p}=102mm, of p-channel MOSFET width). Hence, this on-chip gate driver would require only about 1.1% of the die area. The capability for dispatching the ordinarily-odious gate drive problem at an increase of die cost of only 1% to 2% is a remarkable side-benefit of implementing the planar current switching MOSFET of aspects of this invention in a standard deep-submicron CMOS integrated circuit foundry process. The inclusion of the >20nF bypass capacitor is more costly. Assuming the IC process has no special very high capacitance per unit area (C/A) capability (such as vertical geometry capacitors or ferroelectric dielectrics like many DRAM processes have, then the highest available C/A is the gate to channel capacitance. Implementing, using this

gate oxide capacitance, a bypass capacitor whose capacitance equals the gate capacitance of the W_n=13,500μm current switching MOSFET requires an area equal to approximately 20% of that of the W_n=13,500μm current switching MOSFET. Again, this is a small price to pay for a virtually effortless way of solving the normally odious gate drive problem in high-speed switchers.

The capability for integrating other functionality on the current-switching MOSFET die by including CMOS circuitry of various types is also enabled by the use of a CMOS IC process for fabricating the devices. These could include various types of analog or digital circuitry that would otherwise require separate IC chips in the various applications. One example of this would be the inclusion of the switcher control circuitry for a power converter (i.e., the analog circuitry that compares the actual V_{out} dc output voltage of the converter to the voltage setpoint value and generates the various primary switching and secondary output synchronous rectifier switching timing signals needed for the operation of the power converter. While this would require additional package pins, the value added in reduced parts count and potential for miniaturization would be substantial. Another example, shown in Figure 2b, would be the inclusion of the "optional ultra-low Q_d diode" to replace the "body diode" (Figure 2a) of a normal vertical-geometry power MOSFET. This "body diode" function is emulated by an active diode-connected p-channel MOSFET (i.e., the gate is connected to the drain). This device structure and its applications were discussed in a previous section. Note that it is possible to include both the gate driver amplifier and active diode-connected p-channel MOSFET "body diode" options at the same time (i.e., as additions to the same planar current switching MOSFET die), as could be other application-specific circuitry. Other applications for the planar current switching MOSFET devices of aspects of this invention could benefit from the addition of specialized circuitry designed to serve the needs of each particular application.

FIGURE CAPTIONS

Figure 1a. [Top] Device structure of a conventional vertical geometry power MOSFET showing lateral electron path through surface n-channel transitioning to vertical path down to drain contact.

Figure 1b. [Bottom] Device structure of n-channel planar/horizontal geometry high-current switching MOSFET of aspects of this invention implemented in a deep-submicron CMOS IC process, showing very short lateral electron path for very low R_{on}. Also illustrated at right is the capability to include p-channel MOSFETs on same die.

Figure 2a. [Left] Equivalent circuit for conventional vertical geometry n-channel MOS power FET device, showing body diode. Note that very large stored diffusion charge, Q_d, in body diode severely limits switching speeds at which it can be used.

Figure 2b. [Right] Equivalent circuit for planar/horizontal geometry power high-current switching MOSFET of aspects of this invention, including optional ultra-low stored charge diode implemented with an active diode-connected p-channel MOSFET for use when "body diode" functionality is required.

Figure 3. Cross-section drawing of planar deep-submicron current switching MOSFET of aspects of this invention including high-current die and package interconnects from source and drain electrodes. Die features are drawn to scale for a 2λ=0.24μm feature size CMOS process, but some package/solder ball dimensions reduced to maintain visibility of die features.

Figures 4A - 4B. Plan view of layout example for planar deep-submicron current switching MOSFET of aspects of this invention drawn to scale for implementation in a 2λ=0.24μm feature size CMOS process. The source/drain and gate poly silicide layers plus the via cuts (small squares) up to the first level metal (M1) are illustrated at the upper left. At the upper right, M1, the first level of interconnect metal, is added, and the via cuts to M2 are shown. At the lower left, M2, the second level of interconnect metal, is added, and the via cuts to M3 are shown. At the lower right, M3, the third level of interconnect metal, dedicated principally to the source plane, is added, and the via cuts to M4 are shown.

Figures 5A – 5B. (Continued from Figure 4). Plan view of layout example for planar deep-submicron current switching MOSFET of aspects of this invention drawn to scale for implementation in a 2λ=0.24μm feature size CMOS process. At the upper left, M3 and the via cuts to M4 are shown, as in Figure 4D. At the upper right, M4, the fourth level of interconnect metal, dedicated principally to the drain plane, is added, and the via cuts to M5 are shown. At the lower left, M5, the fifth and final level of interconnect metal, used principally for the source, drain and gate solder ball pads and gate interconnect lines, is added (the scale does not permit showing

the "pad mask" dielectric opening that defines the circular solder ball contact areas). At the lower right, the scale has been changed to show the entire 4mm x 4mm die, showing the M5 (top metal) source, drain and gate solder ball pads with gate interconnect lines running in between them, and the "pad mask" dielectric opening that defines the circular solder ball contact areas.

Figures 6A and 6B. Plan view [top] and cross-sectional view [bottom] of example of a planar package for the planar deep-submicron current switching MOSFET of aspects of this invention. Because the high current (e.g., 200 amp) source and drain leads are coplanar on the package bottom (as well as the ends of the top surface), it would be suitable for surface mount applications (with an appropriate gate lead extension from the gate pad on the top surface).

Figure 7. Example of including optional two CMOS inverter stage gate driver amplifier on the same die as a 200 amp planar deep-submicron current switching MOSFET of aspects of this invention. The driver-amplifier would be capable of supplying 20 to 30 amp gate pulses to the W=13,500mm [$(C_{gs}+C_{gd})$=20nF] planar switching MOSFET for 1.5 to 2ns risetimes of the 0 to 2.5V gate voltage, while presenting only about a 4.5pF capacitive load at the package gate input and requiring less than 1.5% to 2% of the die area.

Figure 8. Example of a gate driver amplifier.

Figures 9A and 9B. Example plan and side views of a vertically laminated package.

Figure 10. 250μm Bump Pitch Calculation of 0.19μm Power Switching FET Resistance with On-Chip Metal and Package R.

Conventional Vertical Power MOSFET Device Structure

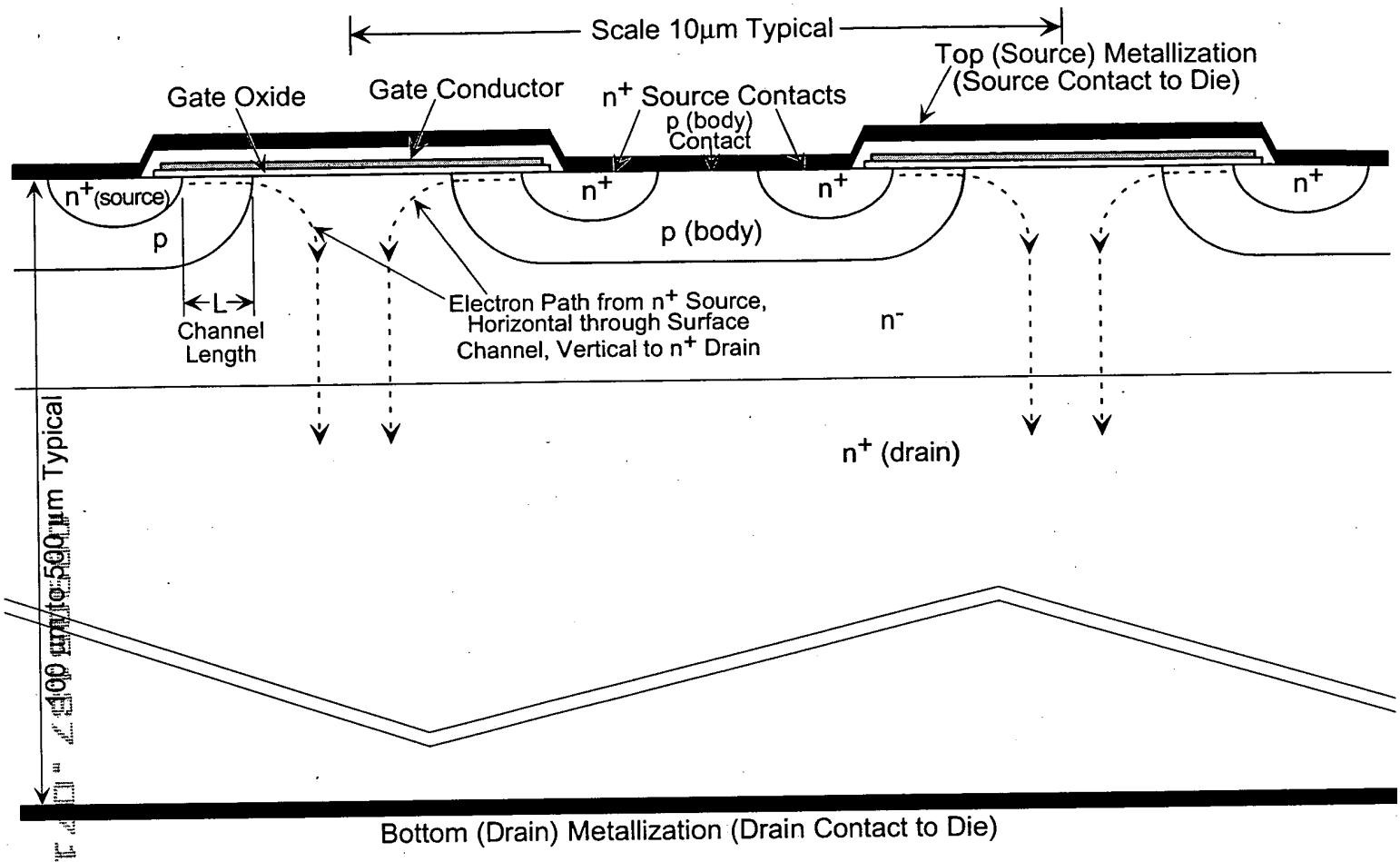


FIG. 1A

CMOS-Implemented Planar Geometry High Current Switching MOSFET Device Structure

Scale 2.0μm Typical

Note: Only M1(1st metal layer) shown; collection of all of the Source, Drain and Gate electrodes into High-Current Source and Drain Chip Contacts on M5 is accomplished in metal layers M2-M5.

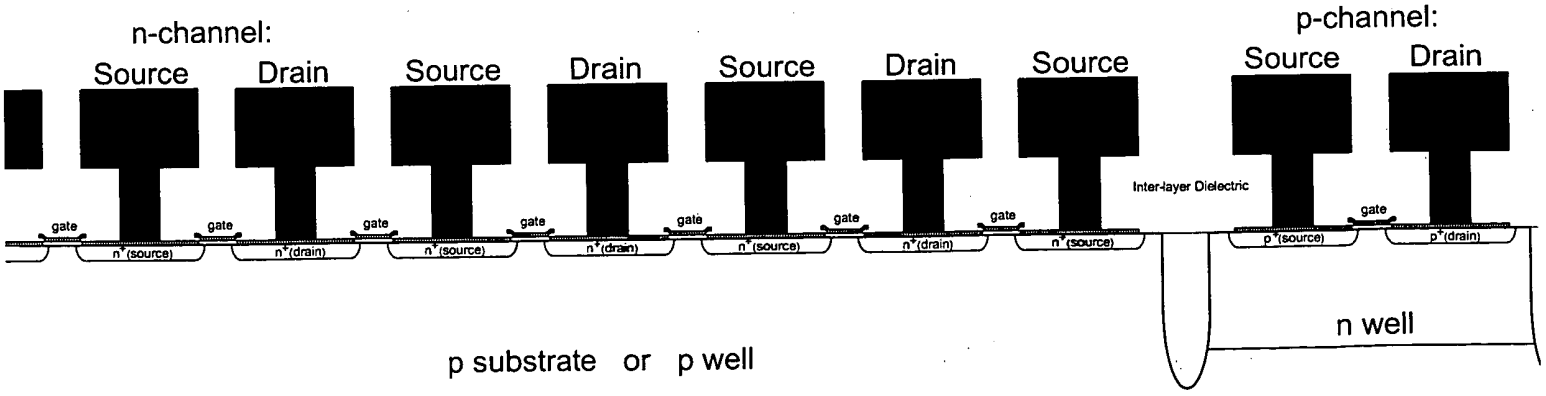
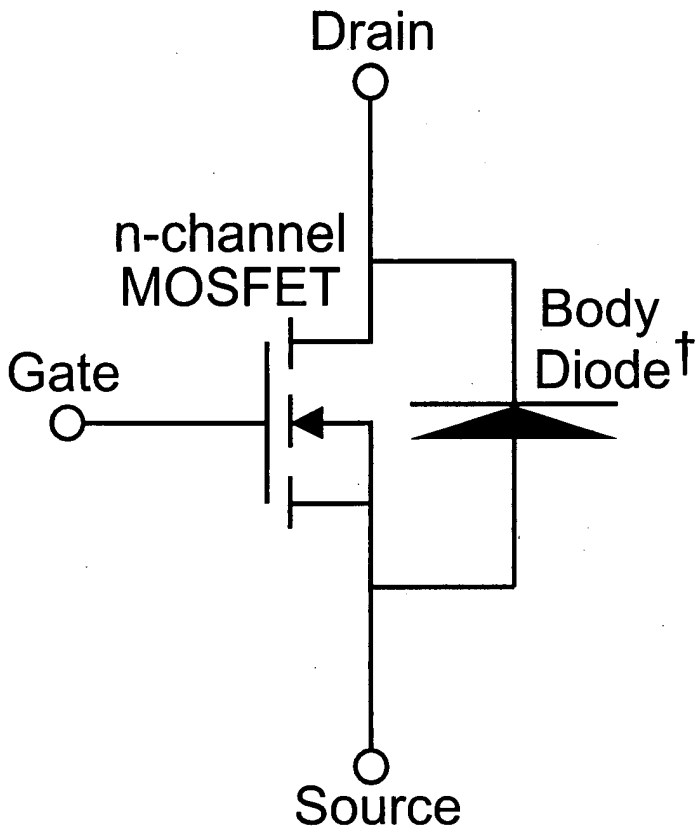


FIG. 1B

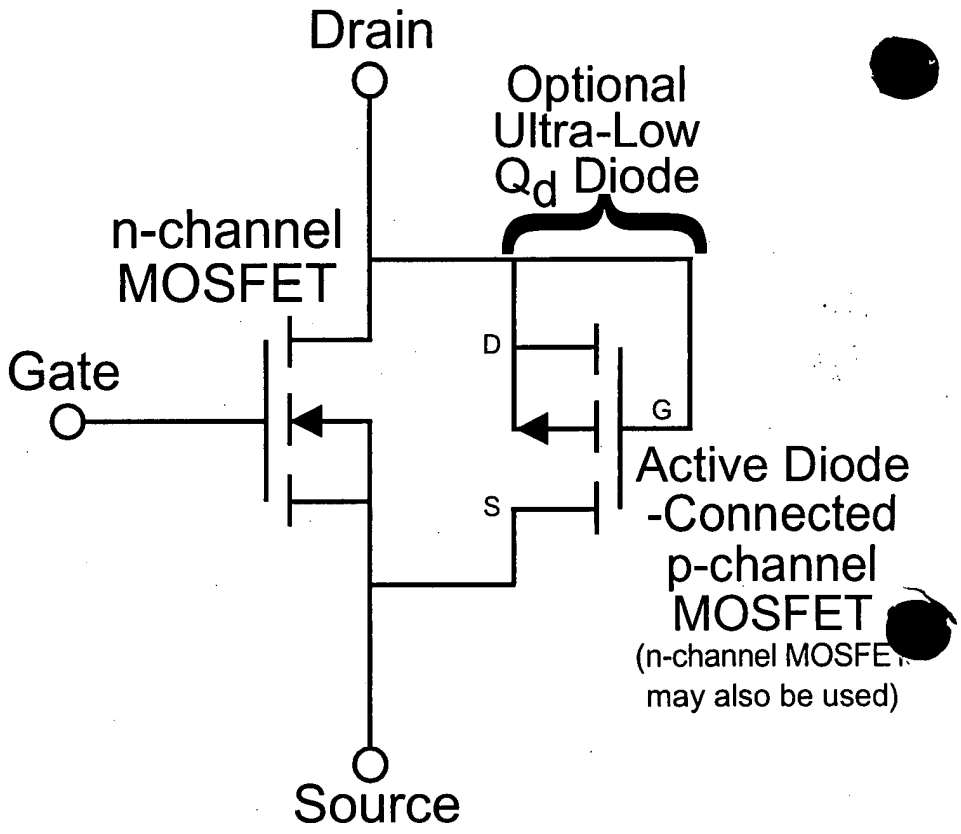
Conventional Power MOSFET Equivalent Circuit



†Note that Body Diode is a very large area p-n$^-$-n$^+$ diode with a very large diffusion charge storage capacity, Q_d. This means that when the body diode is first reverse biased after heavy forward conduction, a large transient reverse current, I_r, can flow for a substantial period of time, $t_r=Q_d/I_r$, which can limit usable switching frequencies.

FIG. 2A

CMOS-Implemented High Current MOSFET Equivalent Circuit



While a p-channel MOSFET with gate connected to Drain is illustrated, an n-channel MOSFET with its gate connected to the Source electrode will also serve as the active "body diode", turning on when the Drain electrode becomes more negative than the Source electrode by an amount greater than the threshold voltage, V_t, of the MOSFET. Note that if the Gate of the switching MOSFET is constrained to go *no* more negative than the Source, then it will, by itself, act as the "body diode".

FIG. 2B

Cross-Section of 200 amp Planar Switching MOSFET Chip and Part of Package

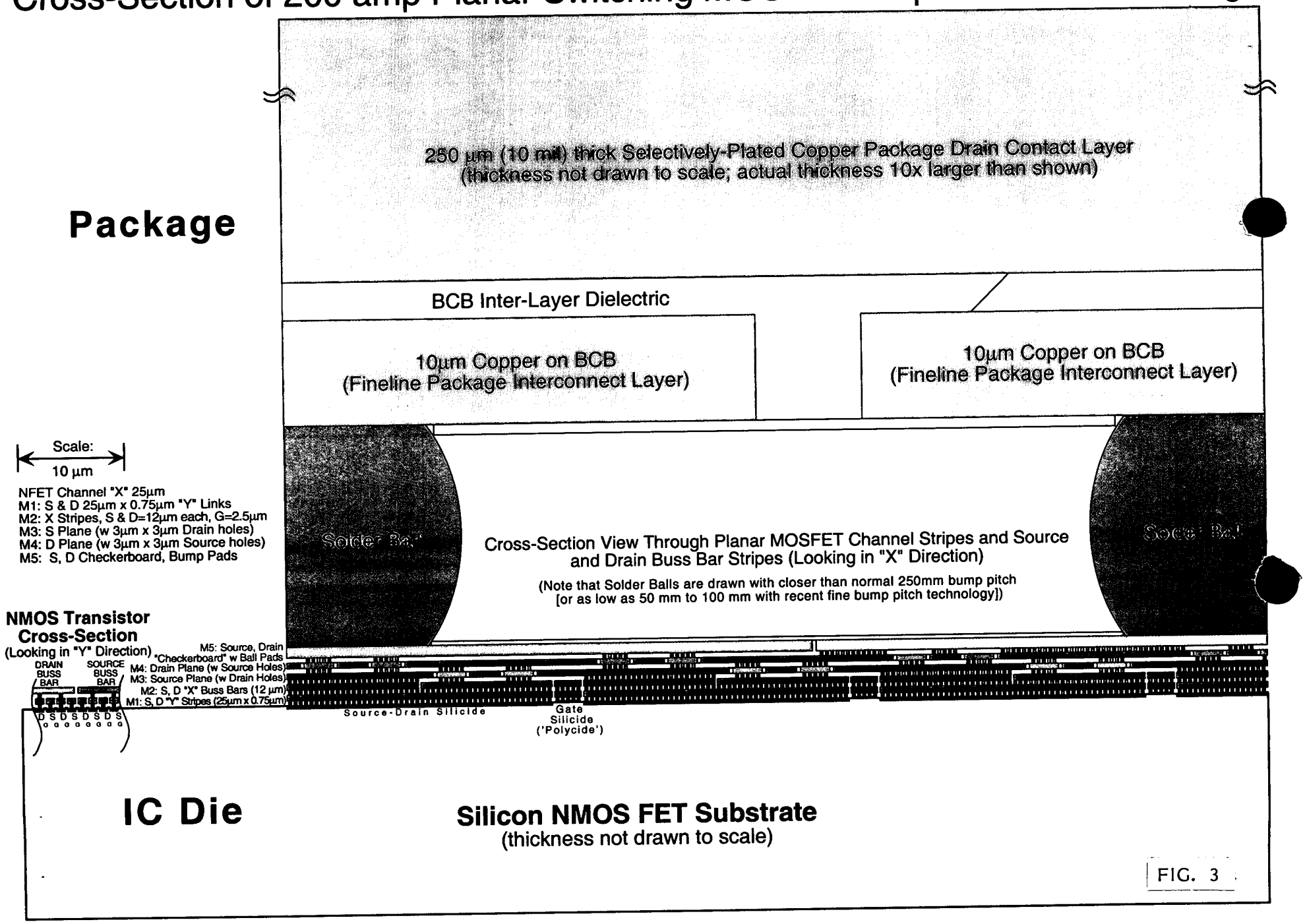
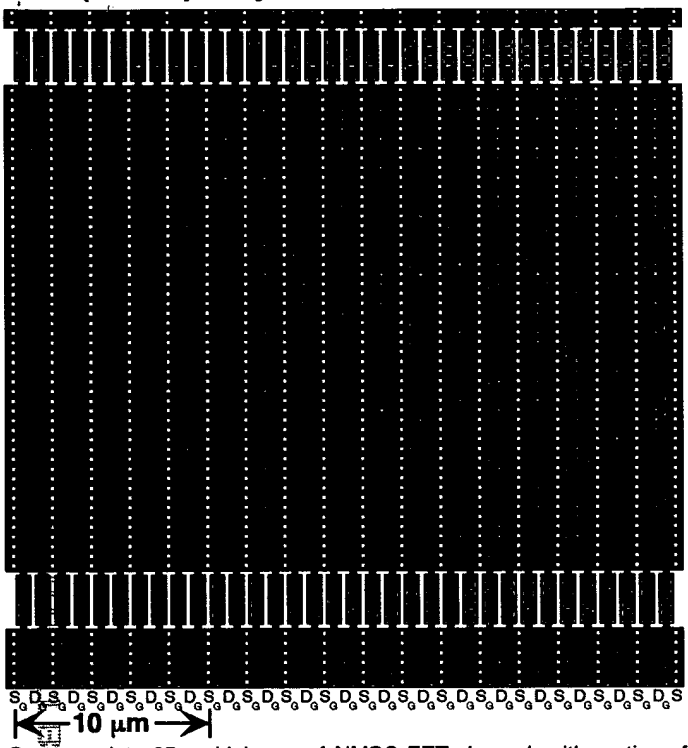


FIG. 3

200 amp NMOS Switching FET Chip; Mask Levels M1-M3 & Poly

FIG. 4A

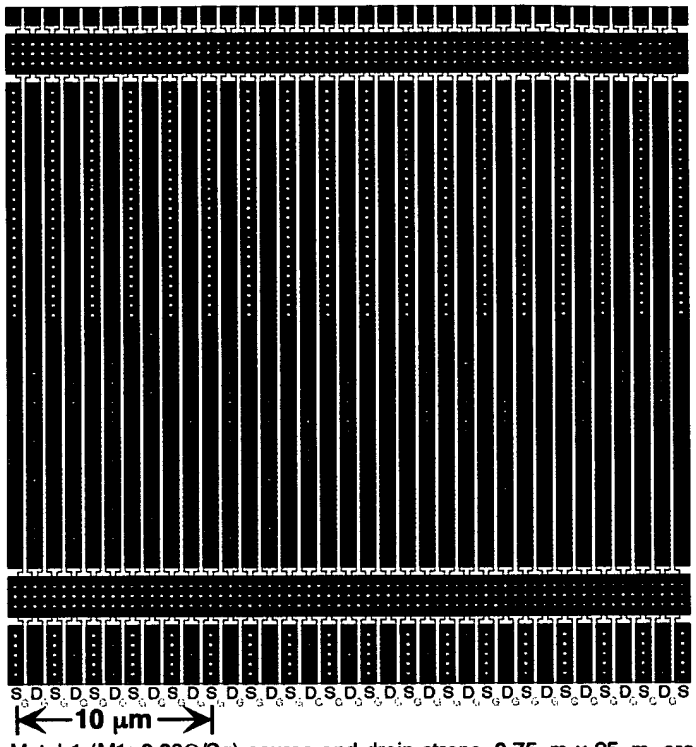
Source (Red)/Drain (Blue) Polysilicide and Gate (Green) Polysilicide with Vias to Metal 1



One complete 25µm high row of NMOS FET channel, with portion of rows above and below, is shown. Each row completes W=250µm of NFET width in 10µm horizontal distance. S/D ohmic contact polysilicide (4Ω/Sq) shown in red for sources, blue for drains, with vias to Metal 1 (7.5Ω/cut) used to reduce current path resistance. Gate polysilicide (7Ω/Sq) is shown in green, with vias to M1 between rows.

FIG. 4B

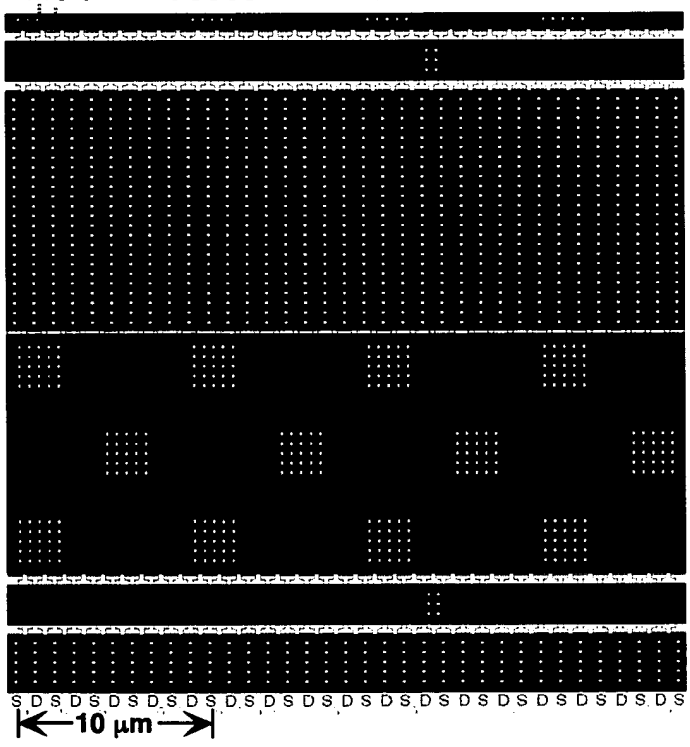
Source (Red), Drain (Blue) and Gate (Green) Metal 1 Jumpers with Vias to Metal 2 Busses



Metal 1 (M1; 0.08Ω/Sq) source and drain straps, 0.75µm x 25µm, are used to reduce resistance of S/D polysilicide in passing current to M2 horizontal S and D busses. Since source M2 buss is taken to cover the upper half of the 25µm channel, the source stripes (red) carry the current from the lower half of the channel to the M1 to M2 vias (5Ω/cut) on the upper half of the channel, and visa-versa for the drain stripes (blue).

FIG. 4C

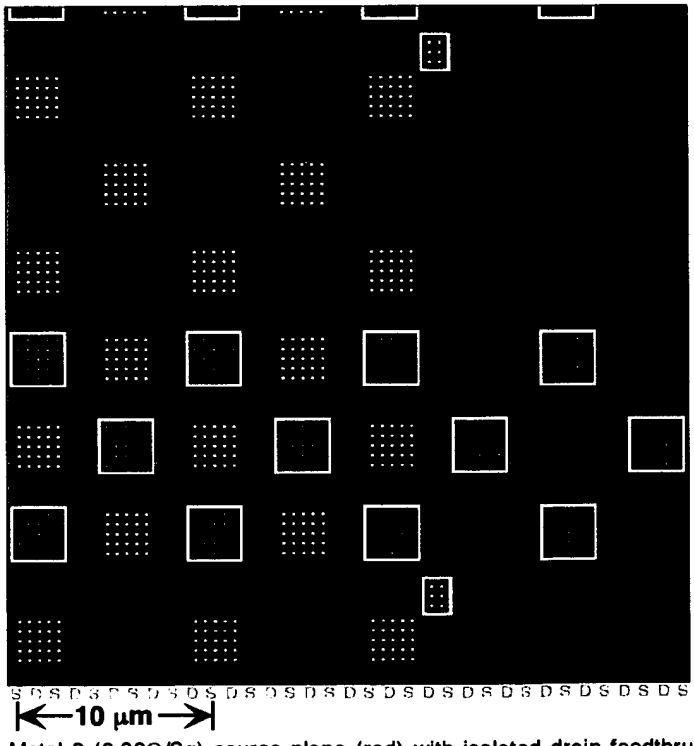
Source (Red), Drain (Blue) and Gate (Green) Metal 2 Busses with Vias to Metal 3 Plane



Horizontal source (red) and drain (blue) M2 (0.08Ω/Sq) busses tie the M1 source and drain stripes together. Since the next, M3, layer is a source plane, the source buss is completely covered with M2/M3 vias (5Ω/cut). The connections from the M2 drain busses to the M4 drain plane are done through an array of isolated M3 patches in the M3 source plane, so the drain buss M2/M3 vias are in patches as shown.

FIG. 4D

Source Metal 3 Plane (Red) & (Blue) Drain M3 Feedthru Patches with Vias to Metal 4 Plane

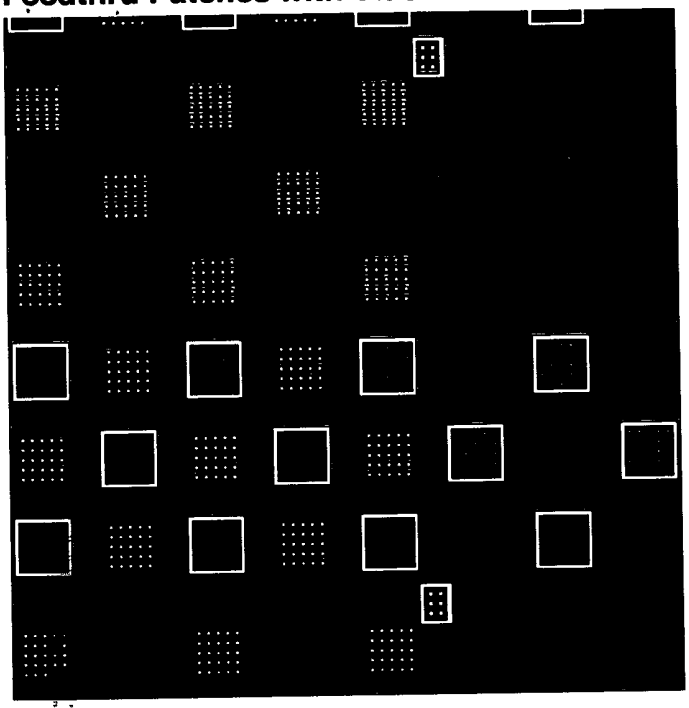


Metal 3 (0.08Ω/Sq) source plane (red) with isolated drain feedthru pads (blue) with M3/M4 via patches carrying current from the M2 drain busses to M4 drain plane. Left 22µm in area shown is under source M5 'checkerboard' pad contact area, so source plane has array of M3/M4 via patches going to isolated feedthru's in M4 drain plane. Right 13µm of area shown has drain M5, so here M3 carries source current laterally.

200 amp NMOS Switching FET Chip: Mask Levels M3-M5 & Ball

FIG. 5A

Source Metal 3 Plane (Red) & (Blue) Drain M3 Feedthru Patches with Vias to Metal 4 Plane

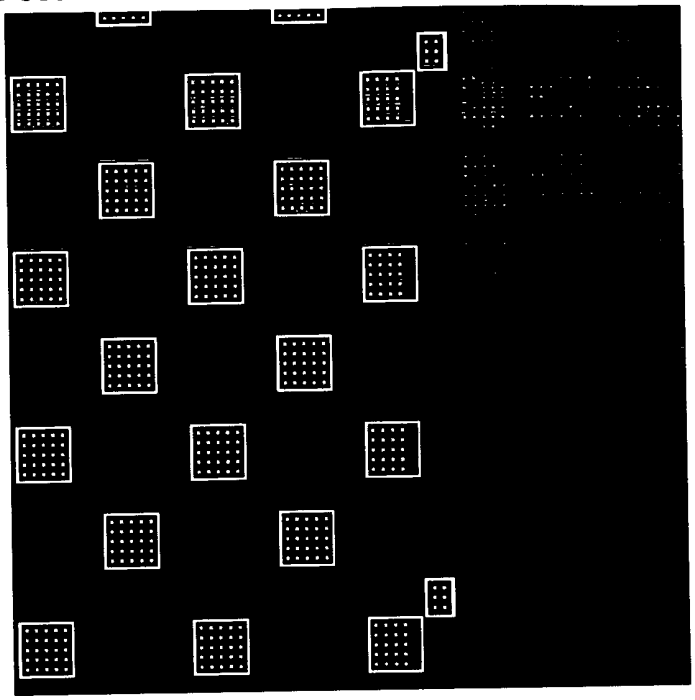


←10 μm→

Metal 3 (0.08Ω/Sq) source plane (red) with isolated drain feedthru pads (blue) with M3/M4 via patches carrying current from the M2 drain busses to M4 drain plane. Left 22μm in area shown is under source M5 'checkerboard' pad contact area, so source plane has array of M3/M4 via patches going to isolated feedthru's in M4 drain plane. Right 13μm of area shown has drain M5, so here M3 carries source current laterally.

FIG. 5B

Drain Metal 4 Plane (Blue) & (Red) Source M4 Feedthru Patches w Vias to Metal 5 Contacts

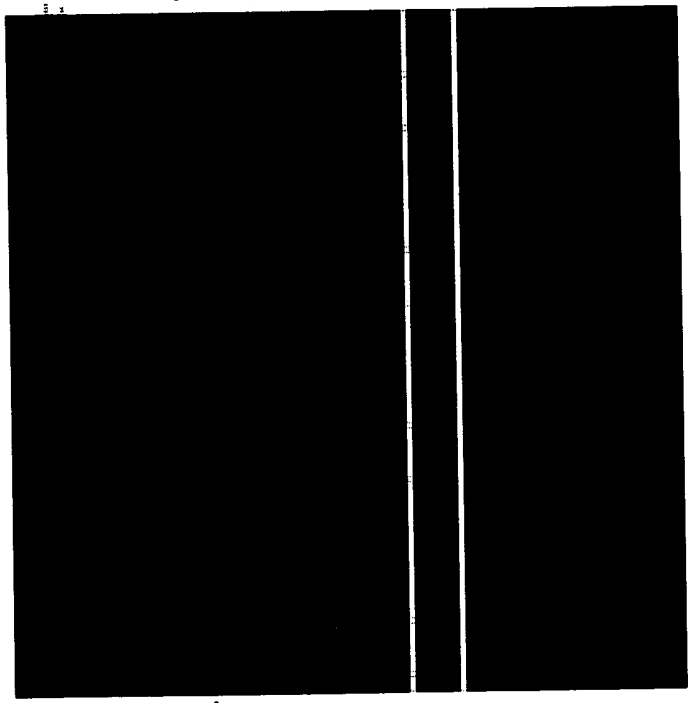


←10 μm→

Metal 4 (0.08Ω/Sq) drain plane (blue) with isolated M4 source feedthru pads (red) with M4/M5 via patches carrying current from the M3 source plane to M5 source 'checkerboard' pad contact area over left 22μm of area drawn. Since right 13μm of area shown has drain M5, this area is covered with M4/M5 vias connecting M4 drain plane with M5 drain pads.

FIG. 5C

Detail of Part of 'Checkerboard' Source (Red) and Drain (Blue) Metal 5 Ball Contact Areas

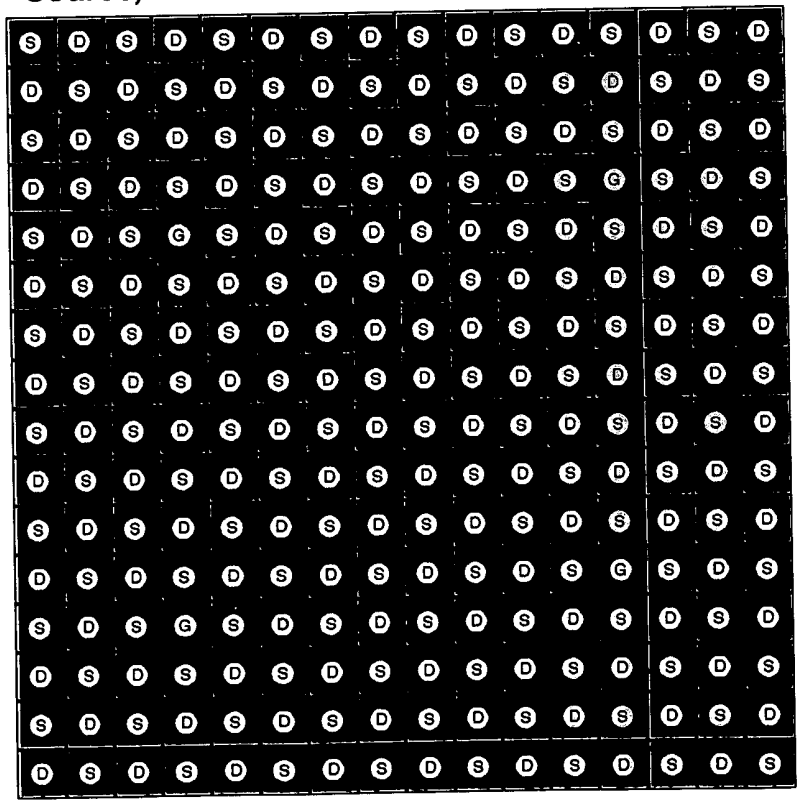


←10 μm→

Small area of Metal 5 (0.04Ω/Sq) ball contact pad 'checkerboard' to same scale as previous drawings. Red area covering left 22μm of drawing is the right side of a source M5 ball contact pad, while the blue area (right 13μm) is the left side of a drain M5 pad. These M5 ball contact pads are nominally 250μm square using standard flip-chip ball pitches, or 100μm or less using advanced 'SHOCC' ball pitches.

FIG. 5D

Full Chip View of Solder Balls and 'Checkerboard' Source, Drain & Gate Metal 5 Ball Contact Areas



←1 mm→

Full chip view of 4mm x 4mm die (scale 100x larger than previous drawings) showing Metal 5 (0.04Ω/Sq) source (red), drain (blue) and gate (green) 'checkerboard' of ball contact pads with solder balls at their centers. While 250μm flip-chip ball pitch is shown, reducing to ≤100μm would improve metal resistance.

FIG. 6A

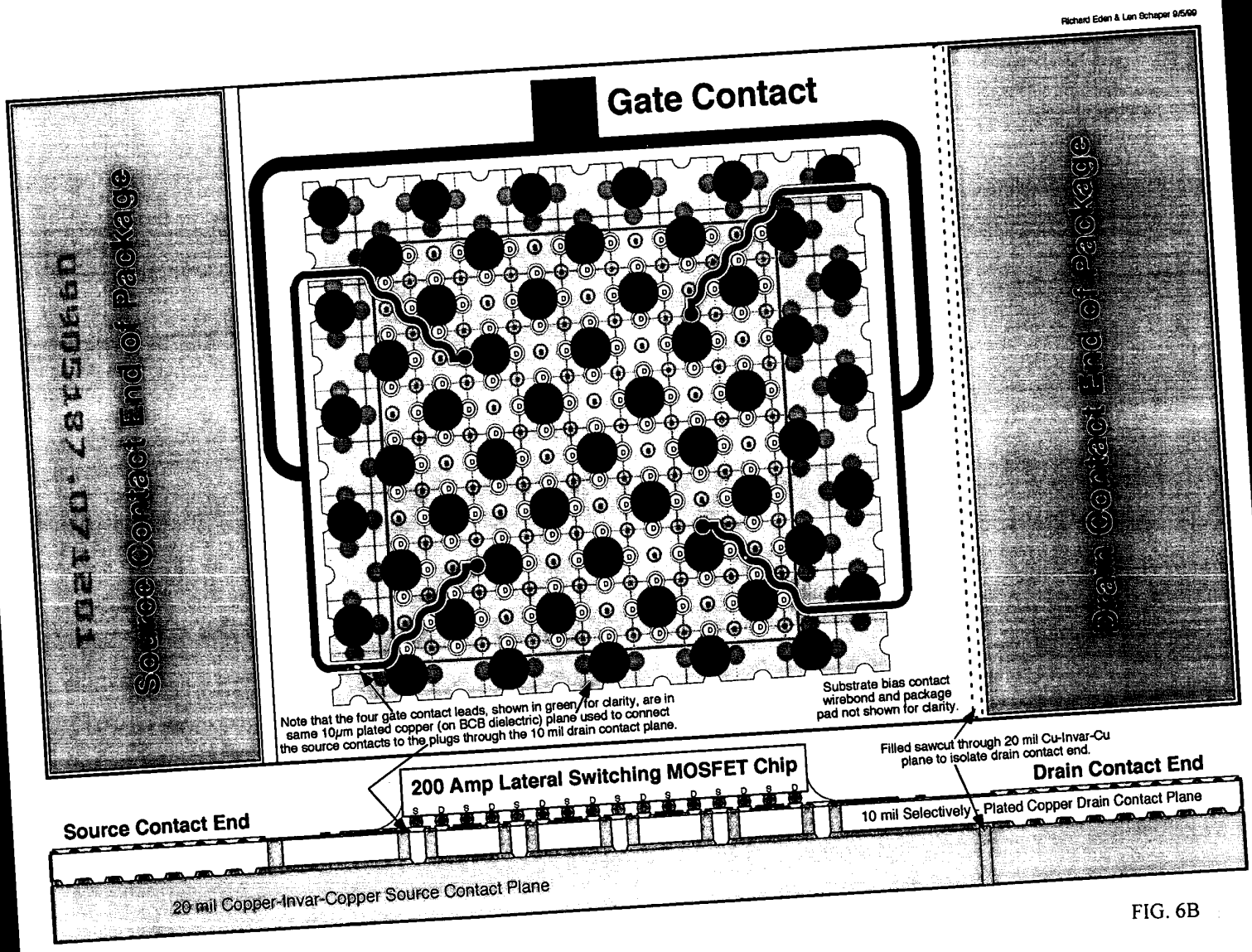

Richard Eden & Len Schaper 9/5/99
Gate Contact
Source Contact End of Package
Drain Contact End of Package
Note that the four gate contact leads, shown in green for clarity, are in same 10μm plated copper (on BCB dielectric) plane used to connect the source contacts to the plugs through the 10 mil drain contact plane.
Substrate bias contact wirebond and package pad not shown for clarity.
Filled sawcut through 20 mil Cu-Invar-Cu plane to isolate drain contact end.
200 Amp Lateral Switching MOSFET Chip
Source Contact End
Drain Contact End
10 mil Selectively Plated Copper Drain Contact Plane
20 mil Copper-Invar-Copper Source Contact Plane

FIG. 6B

Cross-Section of 200 Amp Planar Switching MOSFET Chip After Full-Wafer Deposition of Additive Copper/Polymer Interconnect Layers on Completed IC Wafer

R. C. Eden 8/25/00

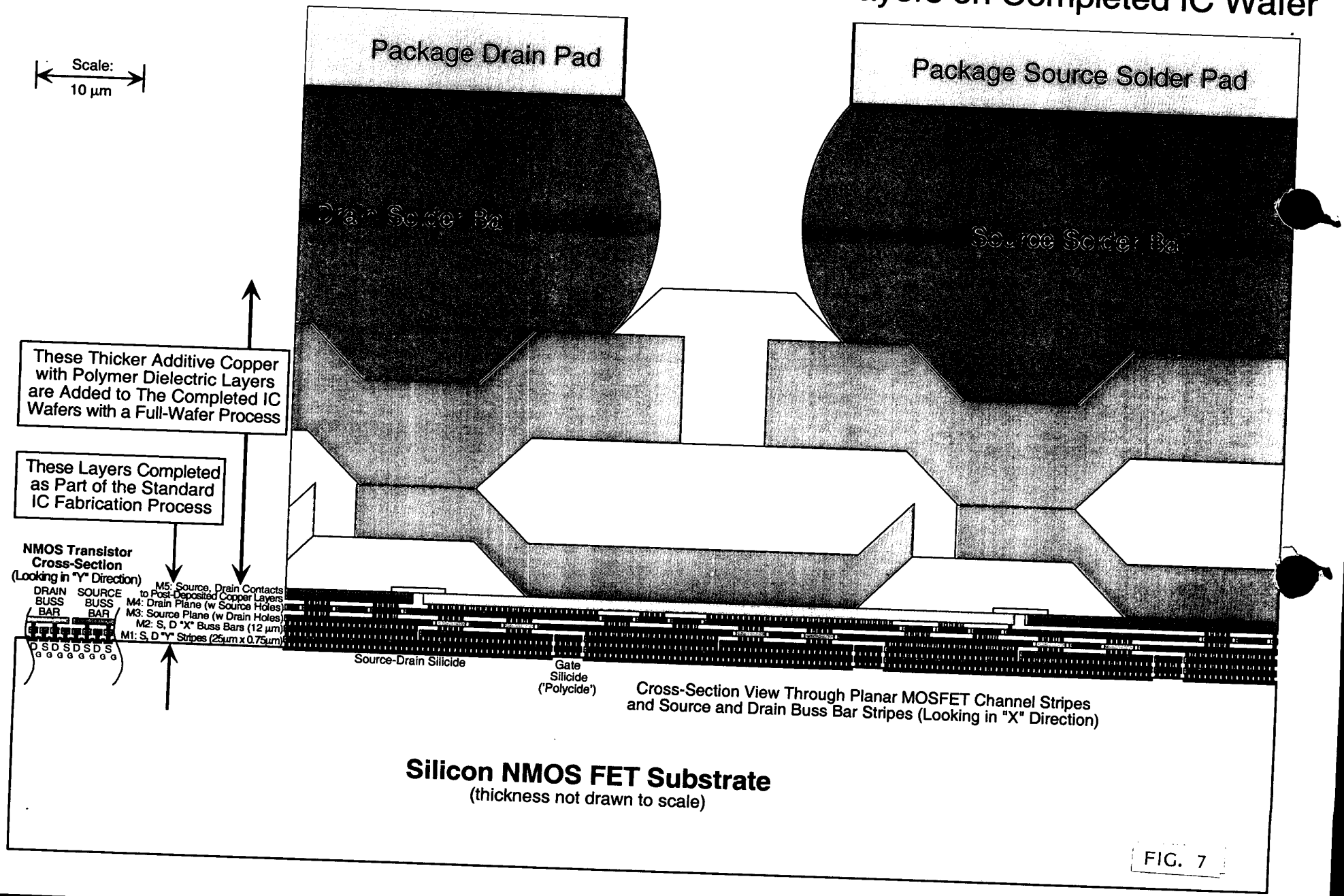


FIG. 7

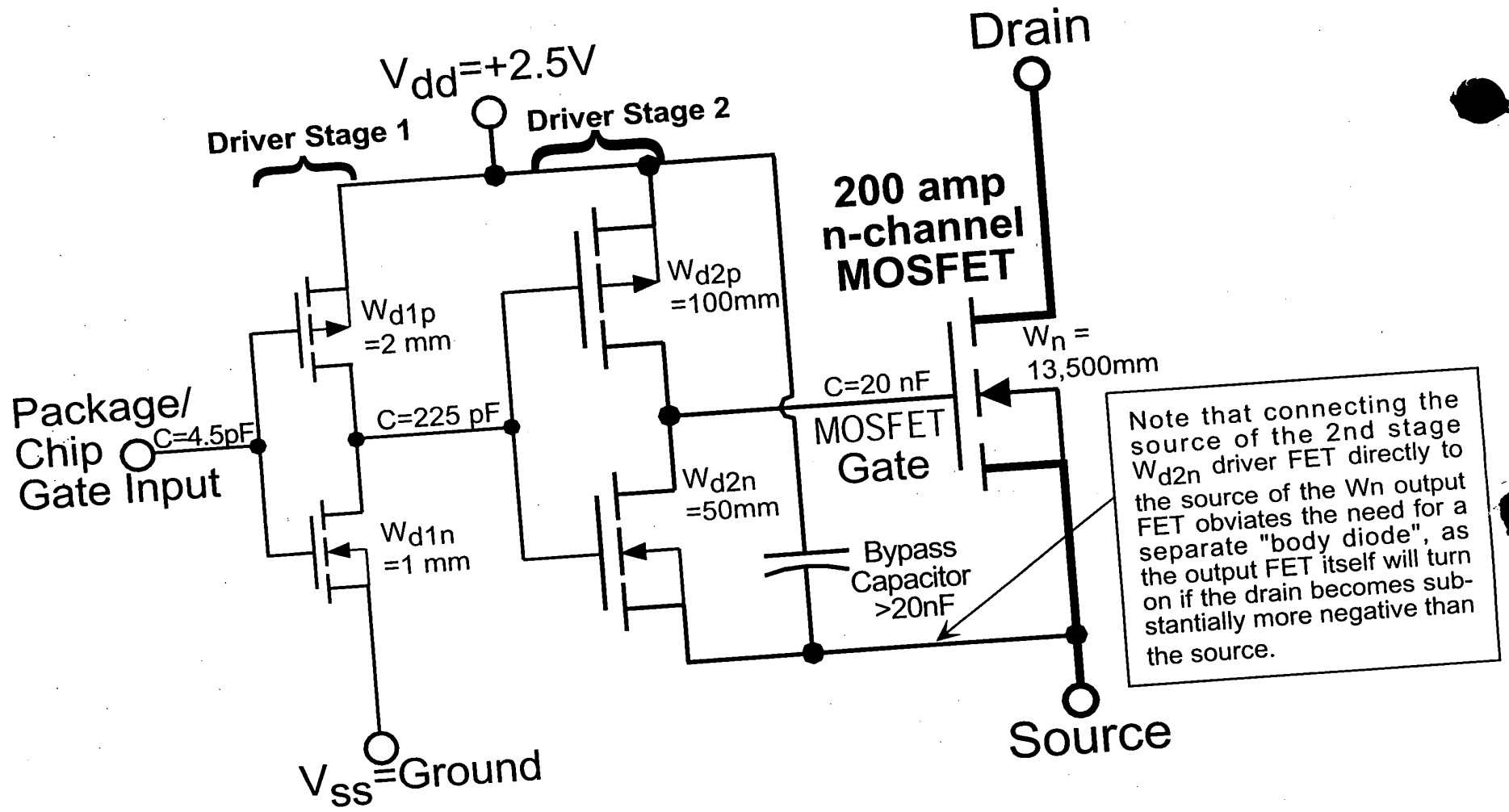


FIG. 8

Alternate "Stripe" Layout of 200 amp NMOS Switching FET Chip with Gate Drive Amplifier for Compatibility with Very Low Resistance Vertically Laminated Package

R. C. Eden 10/8/00

Full Chip View of Solder Balls and Source, Drain & Gate Metal 5 Ball Contact Areas

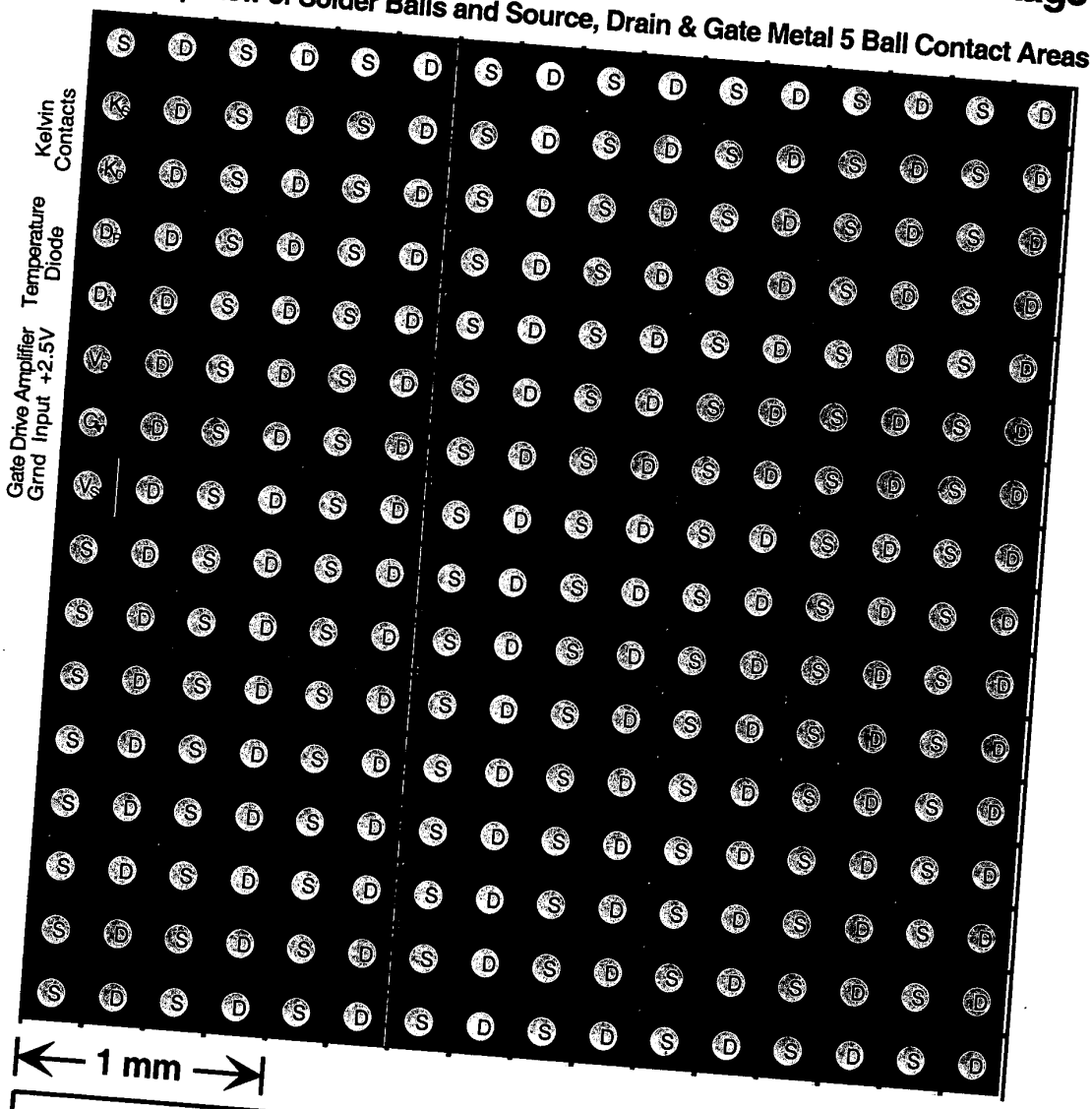
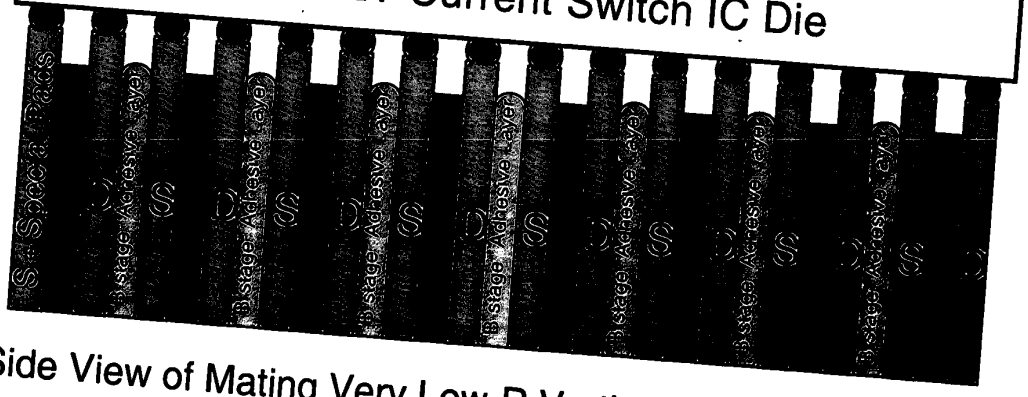


FIG. 9A

MOSFET Current Switch IC Die



Package Height may be Increased Indefinitely for Lower Package Resistance

Side View of Mating Very Low-R Vertical Laminate Package

FIG. 9B

T027.70" 28T50660

250μm Bump Pitch Calculation of 0.18μm Power Switching FET Resistance with On-Chip Metal and Package R

Richard C. Eden 9/14/99

NFET Channel X 25μm M1: S & D 25μmx1μm Y Links M2: X Stripes, S & D=24μm each, G=2.5μm M3: S Plane (w 5x15 D h's) M4: D Plane (w S h's) M5: S, D Pad Checkerboard

Total Channel W=	12.5	meters	12500000	μm
Lambda (Lgd/2)=			0.125	μm
Source/D Width=	6	Lambda	0.75	μm
Source/D Stripe=			25	μm
Gate Stripe W=			3	μm
Vertical Pitch Py=			28	μm
Horizontal Pitch Px=			2	μm
FET Ch W in Pitch Wp=			50	μm
Nominal FET Die Area=	14	mm^2	14000000	(μm)^2
Square Die Size=	3.74166	mm	3741.6574	μm
Drain Via Patch x=			2.5	μm
D Via Patch Pitch Xp=			5	μm
Drain Via Patch y=			2.5	μm
# of Vias per Patch=			25	Vias/Patch
Sheet R for M1-M4			0.08	Ω/Sq
Sheet R for M5			0.04	Ω/Sq
Solder Ball Resistivity	2.2E-05	Ω-cm	22	μΩ-cm
Solder Ball Sheet R	0.00293	Ω/Sq	0.0029333	Ω/Sq
Actual Chip Size=	4	mm		
Ball Pitch=	0.25	mm	250	μm
Number Balls on Chip	16	Balls/Row	256	Balls/chip
Equiv M5 R2/R1 ratio			2	
Equiv Ball R2/R1 ratio			2	
Copper Resistivity	1.7E-06	Ω-cm	1.7	μΩ-cm
Number Cu/BCB Layers			1	Layer(s)
Cu on BCB Thickness	0.001	cm	10	μm
Cu on BCB Sheet R	0.0017	Ω/Square	1.7	mΩ/Sq
Thick Plated Cu Tm	0.0254	cm	10	mils
Thick Plated Cu Sheet F	6.7E-05	Ω/Square	0.0668291	mΩ/Sq
Source Via Plug Dia	0.01524	cm	6	mils
Diagonal Plug Pitch	0.70711	mm	17.960512	mils
Total Package Length	1.26	cm	0.492126	inches
Effective Plane Lpe=	0.5	cm	5	mm
Package Width, Wp=	0.8	cm	0.3149606	inches
Cu-Invar-Cu Substr Tm	0.0508	cm	20	mils
Cu-Invar-Cu Sheet R	3.3E-05	Ω/Square	0.0334646	mΩ/Sq

0.5 μm Aluminum
1.0μm Aluminum
Thickness=0.3 ball pitch

DC Resistance Results Summary:

	Source μΩ	Drain μΩ	Total S+D μΩ		
Silicon/Transistor:	38.40	38.40	76.80		76.8
On-Chip Metallization:	50.49	51.95	102.44		102.43982
Package Metal:	65.53	52.33	117.86		117.86174
Total SI+Metal+Package Resistance:	154.41	142.69	297.10	Micro-Ohms	297.10156
200 Amp 50% DC Power (W)=	3.088	2.854	5.942	Watts	
			2.48%	Loss at Vout=1.2V	

Calculated for Package Conditions: Ball Pitch (μm)= 250
Number of Copper/BCB Layers= 1
Thick Plated Cu Drain Plane Tm(mils)= 10
Via Stud Diagnol Pitch (mils)= 17.9606
Total MOSFET Width (meters)= 12.5

Thickness (μm)= 10
or Tm(μm)= 254
Diameter(mils)= 6
% 4x4 die area= 87.50%

Resistance Component	Symbol	Key Parameter	Parameter Units			Source Portion		Drain Portion		Total (S+D)	Resistance Ohms	Resistance Micro-ohms	Integrated Resistance Micro-ohms	Explanation Conservative Nominal Difference
Silicon/Transistor														
Channel	Rch	580	Ω-μm	at Vgs(V)=	2.5	Rch/2 =	0.0000232	Rch/2 =	0.0000232	Rch=	0.0000464	46.4	46.4	-
Source, Drain	Rs, Rd	190	Ω-μm			Rs =	0.0000152	Rd=	0.0000152	Rs + Rd=	0.0000304	30.4	76.8	-
On-Chip Metallization														
S/D Silicide (Mo)	R(Mo)	4	Ω/Sq	0.375	μm	RSMo=	0.00000012	RDMo=	0.00000012	Rs+d(Mo)=	0.00000024	0.24	77.04	-
Silicide-M1 Via	RV01	7.5	Ω/Cut	12500000	Cuts	RVo1s=	0.0000006	RV01d=	0.0000006	RV01s+d=	0.0000012	1.2	78.24	-
M1 Stripe (S,D)	RM1	0.08	Ω/Sq	250000	16.66666667	RM1s=	2.66667E-06	RM1d=	2.66667E-06	RM1s+d=	5.33333E-06	5.333333333	83.57333333	Only half of the S or D
M1-M2 Via (S,D)	RV12	5	Ω/Cut	6250000	Cuts	RV12s=	0.0000008	RV12d=	0.0000008	RV12s+d=	0.0000016	1.6	85.17333333	
M2 S, D Stripe	RM2	0.08	Ω/Sq			RM2s=	0	RM2d=	0.000001	RM2s+d=	0.000001	1	86.17333333	x1.5 is for Diagonal drain pat
M2-M3 Via (S)	RV23s	5	Ω/Cut	25000000	Cuts	RV23s=	0.0000002			RV23s=	0.0000002	0.2	86.37333333	Could Actually Get in 2x mor
M2-M3 Via (D)	RV23d	5	Ω/Cut	160000	Patches	3750000		RV23d=	1.33333E-06	RV23d=	1.33333E-06	1.333333333	87.70666667	
M3-M4 Via (D)	RV 34d	5	Ω/Cut	150000	Patches			RV34d=	1.33333E-06	RV34d=	1.33333E-06	1.333333333	89.04	
M3-M4 Via (S)	RV34s	5	Ω/Cut	300000	Patches	RV34s=	6.66667E-07			RV34s=	6.66667E-07	0.666666667	89.70666667	Assume same patch pattern
M4-M5 Via (S)	RV45s	5	Ω/Cut	150000	Patches	RV45s=	1.33333E-06			RV45s=	1.33333E-06	1.333333333	91.04	Straight through to M5 under
M4 Spread to M5 (D)	RM4d	0.0571429	M4|M2 Ω/Sq	0.02352941	128			RM4d=	3.35759E-05	RM4d=	3.35759E-05	33.57593395	124.6159239	Assume 40% area coverage
M3 Spread to M5 (S)	RM3s	0.0571429	M3|M2 Ω/Sq	0.02352941	128	RM3s=	3.35759E-05			RM3s=	3.35759E-05	33.57593395	158.1918579	
M5 Spread to Ball (D)	RM5d	0.0236294	M5|M4|.5M2	0.00260818	128			RM5d=	1.0524E-05	RM5d=	1.0524E-05	10.52397587	168.7158338	
M5 Spread to Ball (S)	RM5s	0.0236294	M5|M3|.5M2	0.00260818	128	RM5s=	1.0524E-05			RM5s=	1.0524E-05	10.52397587	179.2398096	
Package/Interconnect													179.2398096	
Solder Ball Resistance	RSB	0.0013446	Ω/Ball	128	Balls	RSBs=	1.05042E-05	RSBd=	1.05042E-05	RSBs+d=	2.10085E-05	21.00845249	200.3482721	Diameter=1/2 Ball Pitch, Hei
Drain Pad Resistance	RSBPd	0	Ω/Pad	128	Drain Ball Pads			RSBPd=	0	RSBPd=	0	0	200.3482721	
Worst Source Pad R	RSPwc	0.0057842	Ω/Pad	25%	5.656854249								200.3482721	x1.26 for 4 stud source pad r
Mid Source Pad R	RSPmc	0.0046274	Ω/Pad	50%	4								200.3482721	
Stud Source Pad R	RSPos	0	Ω/Pad	25%	1								200.3482721	
Average Source Pad R	RSPavg	0.0037597	Ω/Pad	128	Source Ball Pads	RSBPs=	2.9373E-05			RSBPs=	2.9373E-05	29.37296891	229.6211229	
Source Stud Resistance	Rstud	0.0002367	Ω/Stud	50	Studs	Rstud s=	4.73427E-06			Rstud s=	4.73427E-06	4.734287774	234.3554006	
Drain Thick Copper R	RTCUd	6.693E-05	Ω/Sq	0.626	(Left)p/Wp			RTCu(d)=	4.18307E-05	RTCu(d)=	4.18307E-05	41.83070866	276.1861094	
Substrate Cu-Invar-Cu	RCICs	3.346E-05	Ω/Sq	0.626		RCICSub(s)=	2.09154E-05			RCICSub=	2.09154E-05	20.91568433	297.1016938	

Total Source+Drain Resistance= 297.1016938 Micro-Ohms

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FIG. 10